

Distributed by:

JAMECO[®]
ELECTRONICS

www.Jameco.com ♦ 1-800-831-4242

The content and copyrights of the attached
material are the property of its owner.

Jameco Part Number 13071TI

CMOS Hex Buffer/Converters

The CD4049UB and CD4050B devices are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as CMOS to DTL/TTL converters and can drive directly two DTL/TTL loads. ($V_{CC} = 5V$, $V_{OL} \leq 0.4V$, and $I_{OL} \geq 3.3mA$.)

The CD4049UB and CD4050B are designated as replacements for CD4009UB and CD4010B, respectively. Because the CD4049UB and CD4050B require only one power supply, they are preferred over the CD4009UB and CD4010B and should be used in place of the CD4009UB and CD4010B in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049UB and CD4050B are pin compatible with the CD4009UB and CD4010B respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049UB or CD4050B, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink-current or voltage conversion, the CD4069UB Hex Inverter is recommended.

Features

- CD4049UB Inverting
- CD4050B Non-Inverting
- High Sink Current for Driving 2 TTL Loads
- High-To-Low Level Logic Conversion
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of $1\mu A$ at 18V Over Full Package Temperature Range; 100nA at 18V and 25°C
- 5V, 10V and 15V Parametric Ratings

Applications

- CMOS to DTL/TTL Hex Converter
- CMOS Current "Sink" or "Source" Driver
- CMOS High-To-Low Logic Level Converter

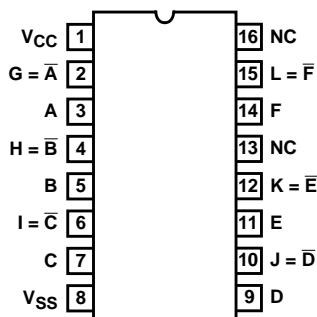
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD4049UBF3A	-55 to 125	16 Ld CERDIP
CD4050BF3A	-55 to 125	16 Ld CERDIP
CD4049UBD	-55 to 125	16 Ld SOIC
CD4049UBDR	-55 to 125	16 Ld SOIC
CD4049UBDW	-55 to 125	16 Ld SOIC
CD4049UBDWR	-55 to 125	16 Ld SOIC
CD4049UBE	-55 to 125	16 Ld PDIP
CD4049UBNSR	-55 to 125	16 Ld SOP
CD4049UBPW	-55 to 125	16 Ld TSSOP
CD4049UBPWR	-55 to 125	16 Ld TSSOP
CD4050BD	-55 to 125	16 Ld SOIC
CD4050BDR	-55 to 125	16 Ld SOIC
CD4050BDW	-55 to 125	16 Ld SOIC
CD4050BDWR	-55 to 125	16 Ld SOIC
CD4050BE	-55 to 125	16 Ld PDIP
CD4050NSR	-55 to 125	16 Ld SOP
CD4050BPW	-55 to 125	16 Ld TSSOP
CD4050BPWR	-55 to 125	16 Ld TSSOP

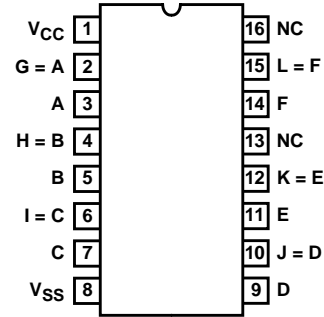
NOTE: When ordering, use the entire part number. The suffix R denotes tape and reel.

Pinouts

CD4049UB (PDIP, CERDIP, SOIC, SOP, TSSOP)
TOP VIEW

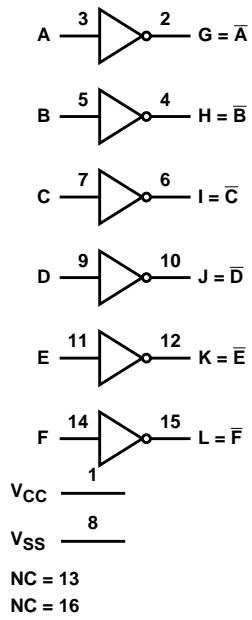


CD4050B (PDIP, CERDIP, SOIC, SOP)
TOP VIEW

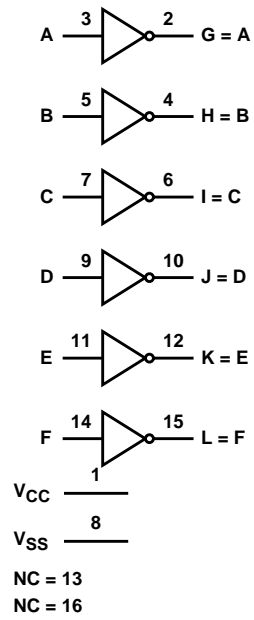


Functional Block Diagrams

CD4049UB



CD4050B



Schematic Diagrams

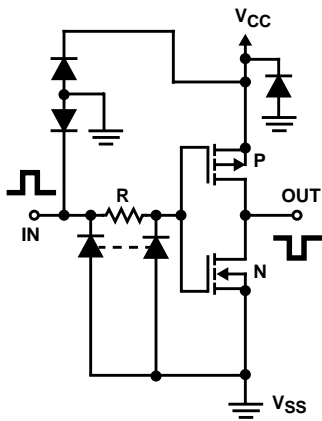


FIGURE 1A. SCHEMATIC DIAGRAM OF CD4049UB, 1 OF 6 IDENTICAL UNITS

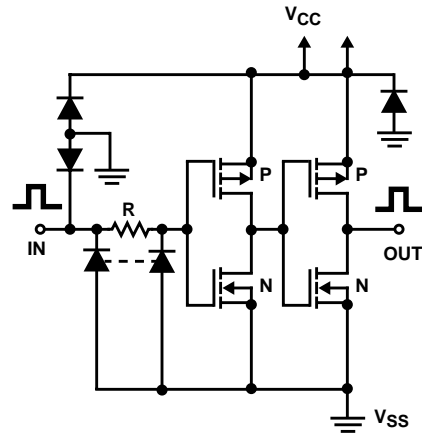


FIGURE 1B. SCHEMATIC DIAGRAM OF CD4050B, 1 OF 6 IDENTICAL UNITS

CD4049UB, CD4050B

Absolute Maximum Ratings

Supply Voltage (V+ to V-) -0.5V to 20V
 DC Input Current, Any One Input ±10mA

Operating Conditions

Temperature Range -55°C to 125°C

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note1):
 E Package 67°C/W
 D Package 73°C/W
 DW Package 57°C/W
 NS Package 64°C/W
 PW Package 108°C/W
 Maximum Junction Temperature (Plastic Package) 150°
 Maximum Storage Temperature Range 65°C to 150°
 Maximum Lead Temperature (Soldering 10s) 265°
 SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURE (°C)							UNITS
				25							
	V _O (V)	V _{IN} (V)	V _{CC} (V)	-55	-40	85	125	MIN	TYP	MAX	
Quiescent Device Current I _{DD} (Max)	-	0,5	5	1	1	30	30	-	0.02	1	µA
	-	0,10	10	2	2	60	60	-	0.02	2	µA
	-	0,15	15	4	4	120	120	-	0.02	4	µA
	-	0,20	20	20	20	600	600	-	0.04	20	µA
Output Low (Sink) Current I _{OL} (Min)	0.4	0,5	4.5	3.3	3.1	2.1	1.8	2.6	5.2	-	mA
	0.4	0,5	5	4	3.8	2.9	2.4	3.2	6.4	-	mA
	0.5	0,10	10	10	9.6	6.6	5.6	8	16	-	mA
	1.5	0,15	15	26	25	20	18	24	48	-	mA
Output High (Source) Current I _{OH} (Min)	4.6	0,5	5	-0.81	-0.73	-0.58	-0.48	-0.65	-1.2	-	mA
	2.5	0,5	5	-2.6	-2.4	-1.9	-1.55	-2.1	-3.9	-	mA
	9.5	0,10	10	-2.0	-1.8	-1.35	-1.18	-1.65	-3.0	-	mA
	13.5	0,15	15	-5.2	-4.8	-3.5	-3.1	-4.3	-8.0	-	mA
Out Voltage Low Level V _{OL} (Max)	-	0,5	5	0.05	0.05	0.05	0.05	-	0	0.05	V
	-	0,10	10	0.05	0.05	0.05	0.05	-	0	0.05	V
	-	0,15	5	0.05	0.05	0.05	0.05	-	0	0.05	V
Output Voltage High Level V _{OH} (Min)	-	0,5	5	4.95	4.95	4.95	4.95	4.95	5	-	V
	-	0,10	10	9.95	9.95	9.95	9.95	9.95	10	-	V
	-	0,15	15	14.95	14.95	14.95	14.95	14.95	15	-	V
Input Low Voltage, V _{IL} (Max) CD4049UB	4.5	-	5	1	1	1	1	-	-	1	V
	9	-	10	2	2	2	2	-	-	2	V
	13.5	-	15	2.5	2.5	2.5	2.5	-	-	2.5	V
Input Low Voltage, V _{IL} (Max) CD4050B	0.5	-	5	1.5	1.5	1.5	1.5	-	-	1.5	V
	1	-	10	3	3	3	3	-	-	3	V
	1.5	-	15	4	4	4	4	-	-	4	V

CD4049UB, CD4050B

DC Electrical Specifications (Continued)

PARAMETER	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURE (°C)							UNITS
				25							
	V _O (V)	V _{IN} (V)	V _{CC} (V)	-55	-40	85	125	MIN	TYP	MAX	
Input High Voltage, V _{IH} Min CD4049UB	0.5	-	5	4	4	4	4	4	-	-	V
	1	-	10	8	8	8	8	8	-	-	V
	1.5	-	15	12.5	12.5	12.5	12.5	12.5	-	-	V
Input High Voltage, V _{IH} Min CD4050B	4.5	-	5	3.5	3.5	3.5	3.5	3.5	-	-	V
	9	-	10	7	7	7	7	7	-	-	V
	13.5	-	15	11	11	11	11	11	-	-	V
Input Current, I _{IN} Max	-	0,18	18	±0.1	±0.1	±1	±1	-	±10 ⁻⁵	±0.1	μA

AC Electrical Specifications T_A = 25°C, Input t_r, t_f = 20ns, C_L = 50pF, R_L = 200kΩ

PARAMETER	TEST CONDITIONS		LIMITS (ALL PACKAGES)		UNITS
	V _{IN}	V _{CC}	TYP	MAX	
Propagation Delay Time Low to High, t _{PLH} CD4049UB	5	5	60	120	ns
	10	10	32	65	ns
	10	5	45	90	ns
	15	15	25	50	ns
	15	5	45	90	ns
Propagation Delay Time Low to High, t _{PLH} CD4050B	5	5	70	140	ns
	10	10	40	80	ns
	10	5	45	90	ns
	15	15	30	60	ns
	15	5	40	80	ns
Propagation Delay Time High to Low, t _{PHL} CD4049UB	5	5	32	65	ns
	10	10	20	40	ns
	10	5	15	30	ns
	15	15	15	30	ns
	15	5	10	20	ns
Propagation Delay Time High to Low, t _{PHL} CD4050B	5	5	55	110	ns
	10	10	22	55	ns
	10	5	50	100	ns
	15	15	15	30	ns
	15	5	50	100	ns
Transition Time, Low to High, t _{TLH}	5	5	80	160	ns
	10	10	40	80	ns
	15	15	30	60	ns
Transition Time, High to Low, t _{THL}	5	5	30	60	ns
	10	10	20	40	ns
	15	15	15	30	ns

CD4049UB, CD4050B

AC Electrical Specifications $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ns}$, $C_L = 50\text{pF}$, $R_L = 200\text{k}\Omega$ (Continued)

PARAMETER	TEST CONDITIONS		LIMITS (ALL PACKAGES)		UNITS
	V_{IN}	V_{CC}	TYP	MAX	
Input Capacitance, C_{IN} CD4049UB	-	-	15	22.5	pF
Input Capacitance, C_{IN} CD4050B	-	-	5	7.5	pF

Typical Performance Curves

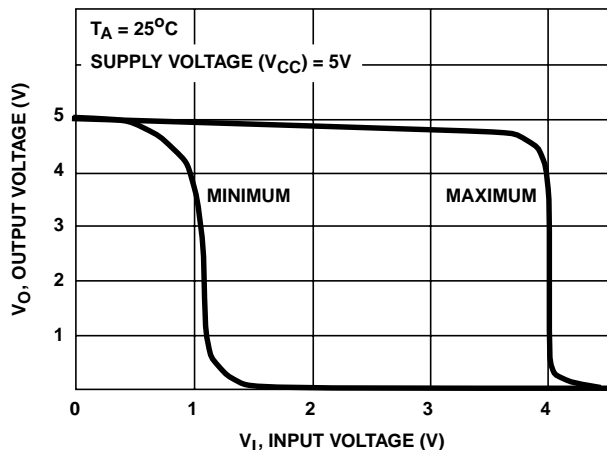


FIGURE 2. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS FOR CD4049UB

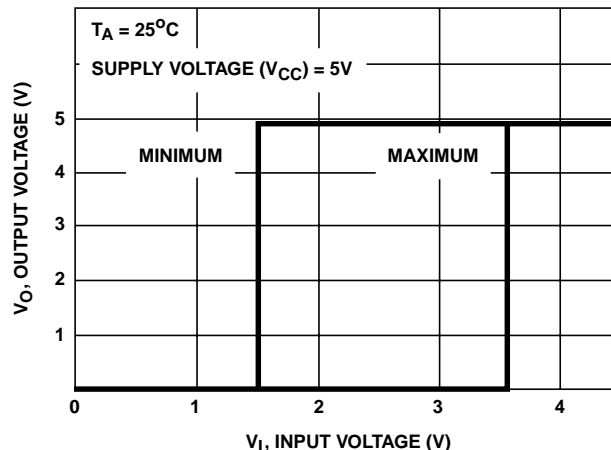


FIGURE 3. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS FOR CD4050B

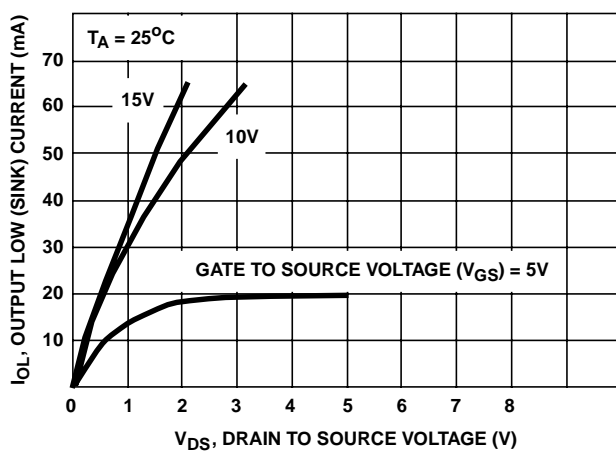


FIGURE 4. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

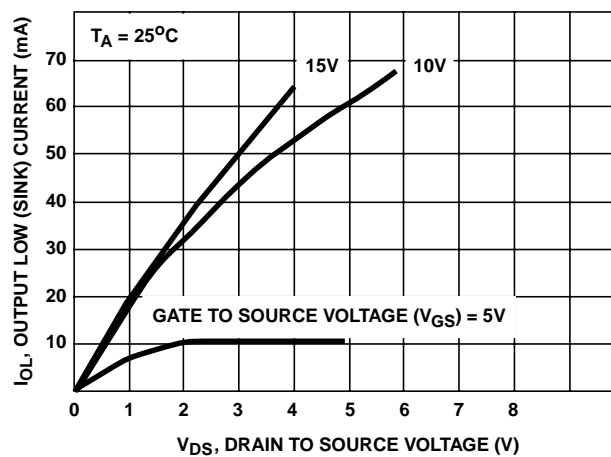


FIGURE 5. MINIMUM OUTPUT LOW (SINK) CURRENT DRAIN CHARACTERISTICS

Typical Performance Curves (Continued)

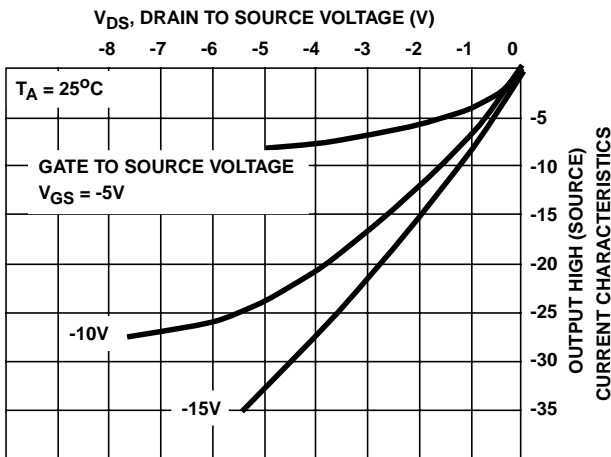


FIGURE 6. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

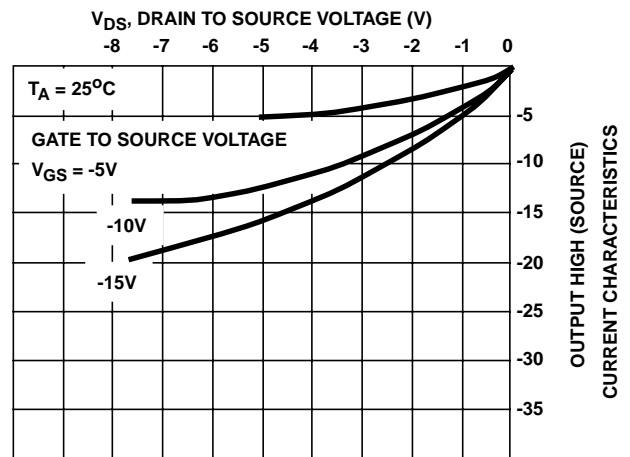


FIGURE 7. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

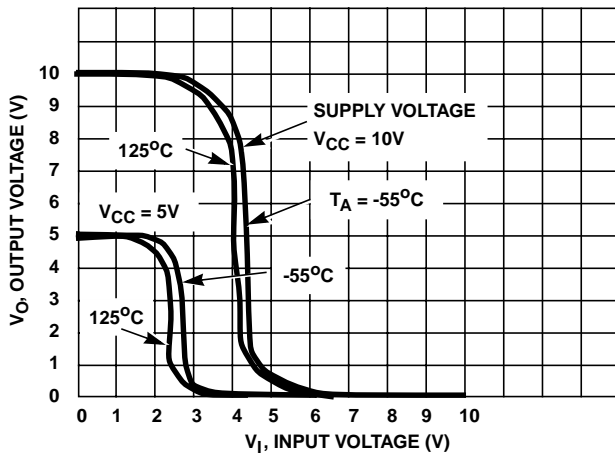


FIGURE 8. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE FOR CD4049UB

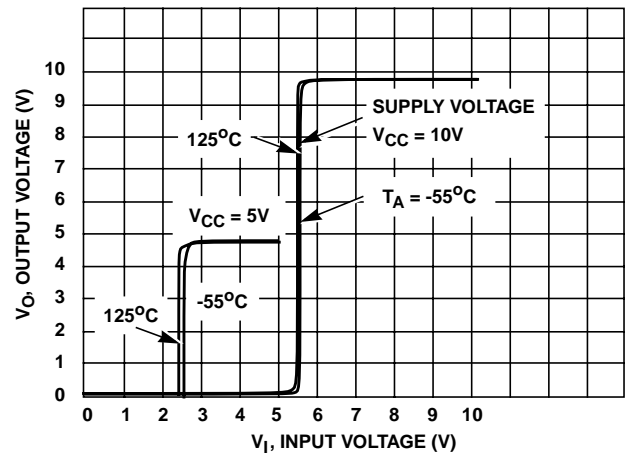


FIGURE 9. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE FOR CD4050B

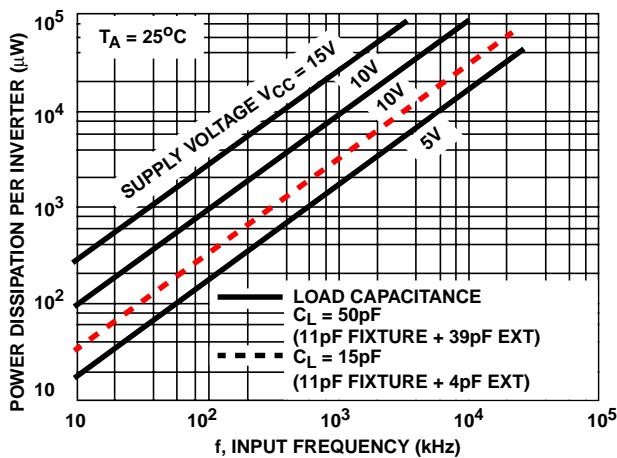


FIGURE 10. TYPICAL POWER DISSIPATION vs FREQUENCY CHARACTERISTICS

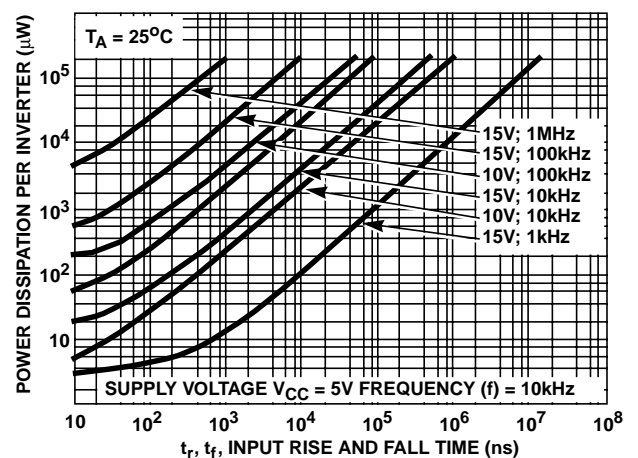


FIGURE 11. TYPICAL POWER DISSIPATION vs INPUT RISE AND FALL TIMES PER INVERTER FOR CD4049UB

Typical Performance Curves (Continued)

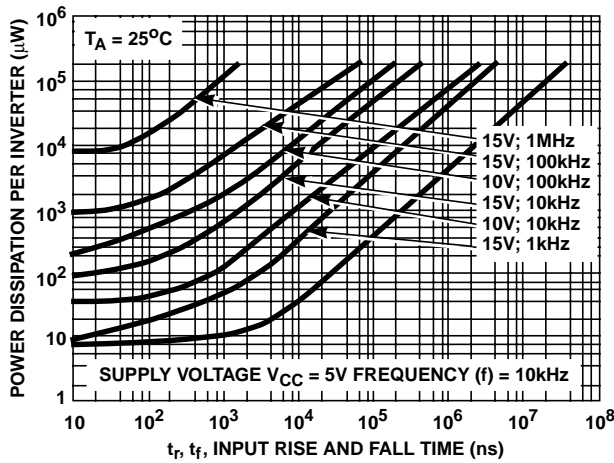


FIGURE 12. TYPICAL POWER DISSIPATION vs INPUT RISE AND FALL TIMES PER INVERTER FOR CD4050B

Test Circuits

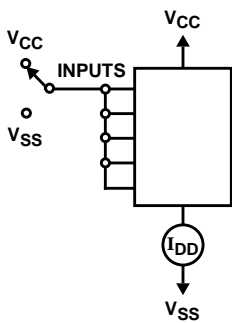
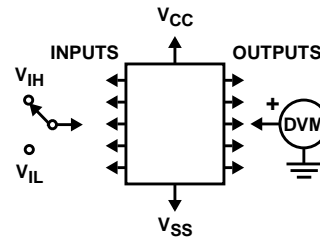
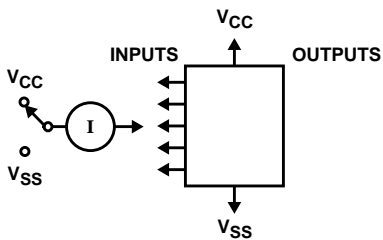


FIGURE 13. QUIESCENT DEVICE CURRENT TEST CIRCUIT



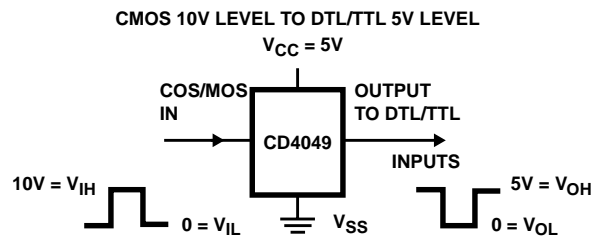
NOTE: Test any one input with other inputs at V_{CC} or V_{SS}.

FIGURE 14. INPUT VOLTAGE TEST CIRCUIT



NOTE: Measure inputs sequentially, to both V_{CC} and V_{SS} connect all unused inputs to either V_{CC} or V_{SS}.

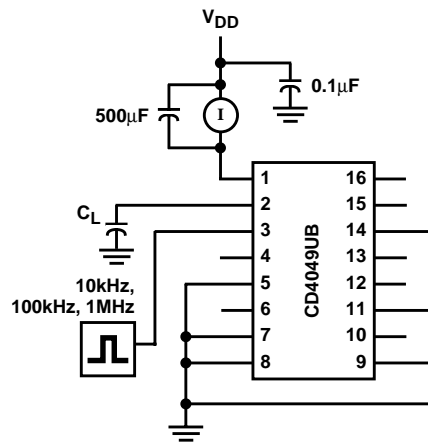
FIGURE 15. INPUT CURRENT TEST CIRCUIT



In Terminal - 3, 5, 7, 9, 11, or 14
Out Terminal - 2, 4, 6, 10, 12 or 15
V_{CC} Terminal - 1
V_{SS} Terminal - 8

FIGURE 16. LOGIC LEVEL CONVERSION APPLICATION

Test Circuits (Continued)



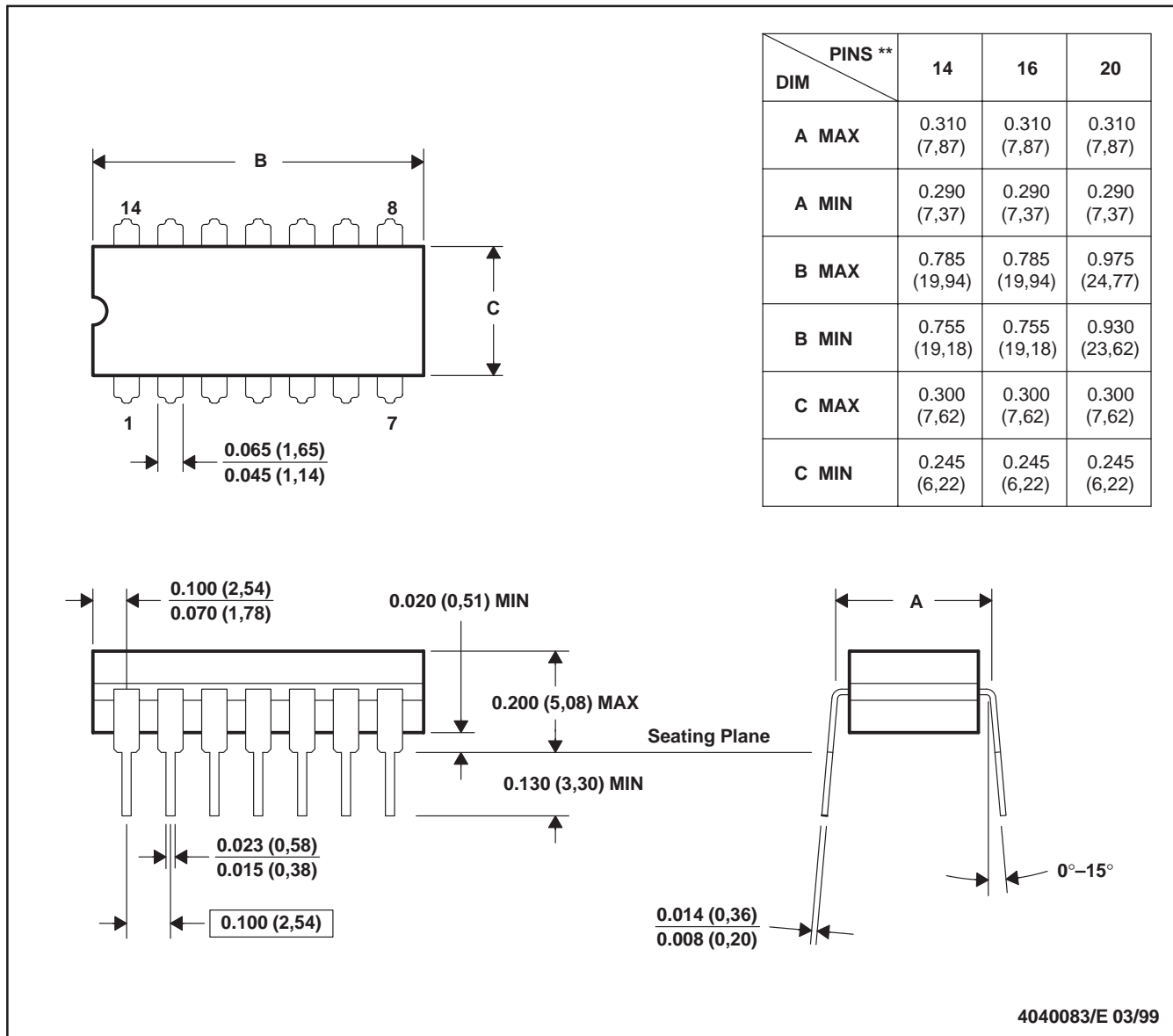
C_L INCLUDES FIXTURE CAPACITANCE

FIGURE 17. DYNAMIC POWER DISSIPATION TEST CIRCUITS

J (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

14 LEADS SHOWN

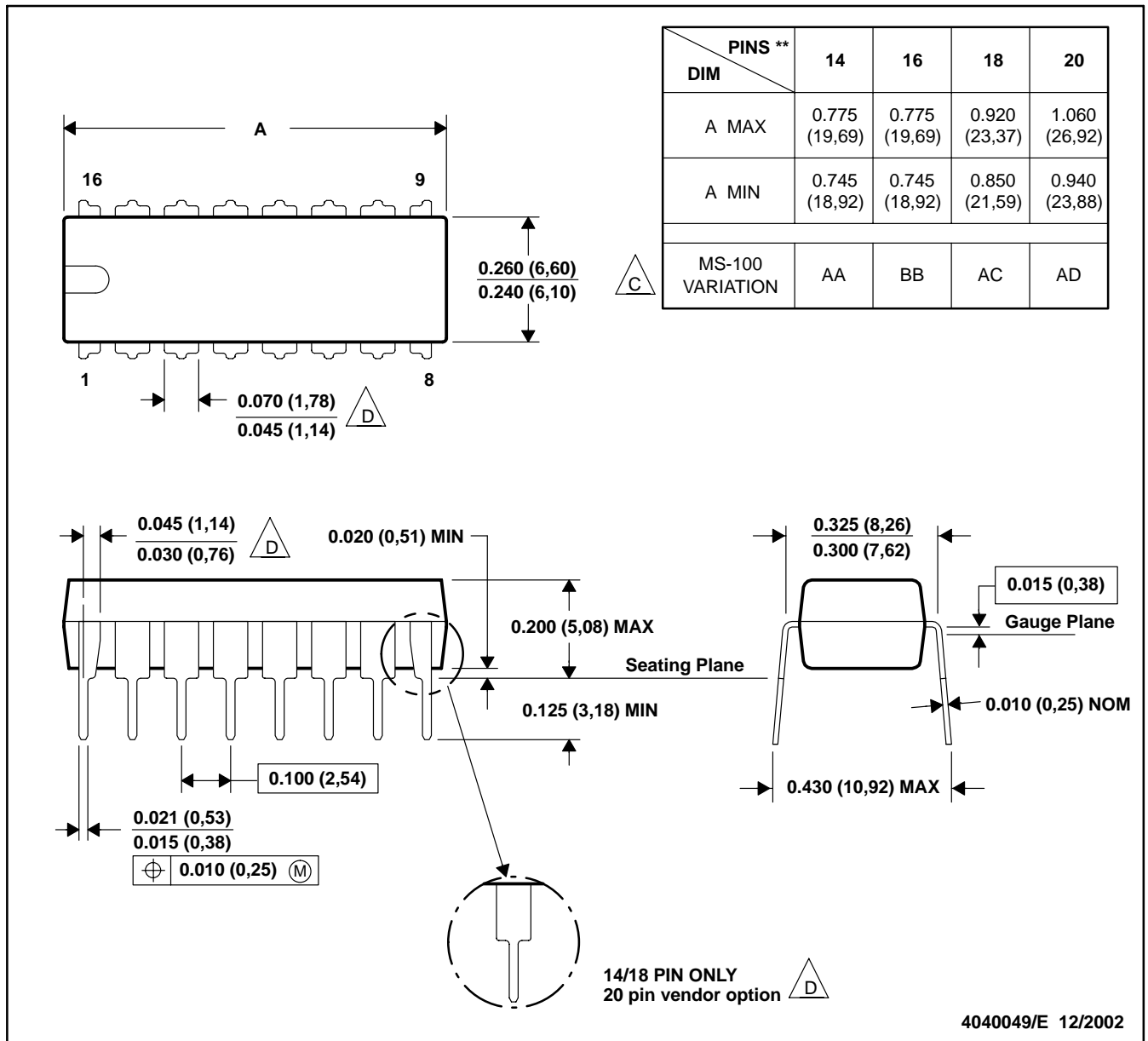


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package is hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, and GDIP1-T20

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

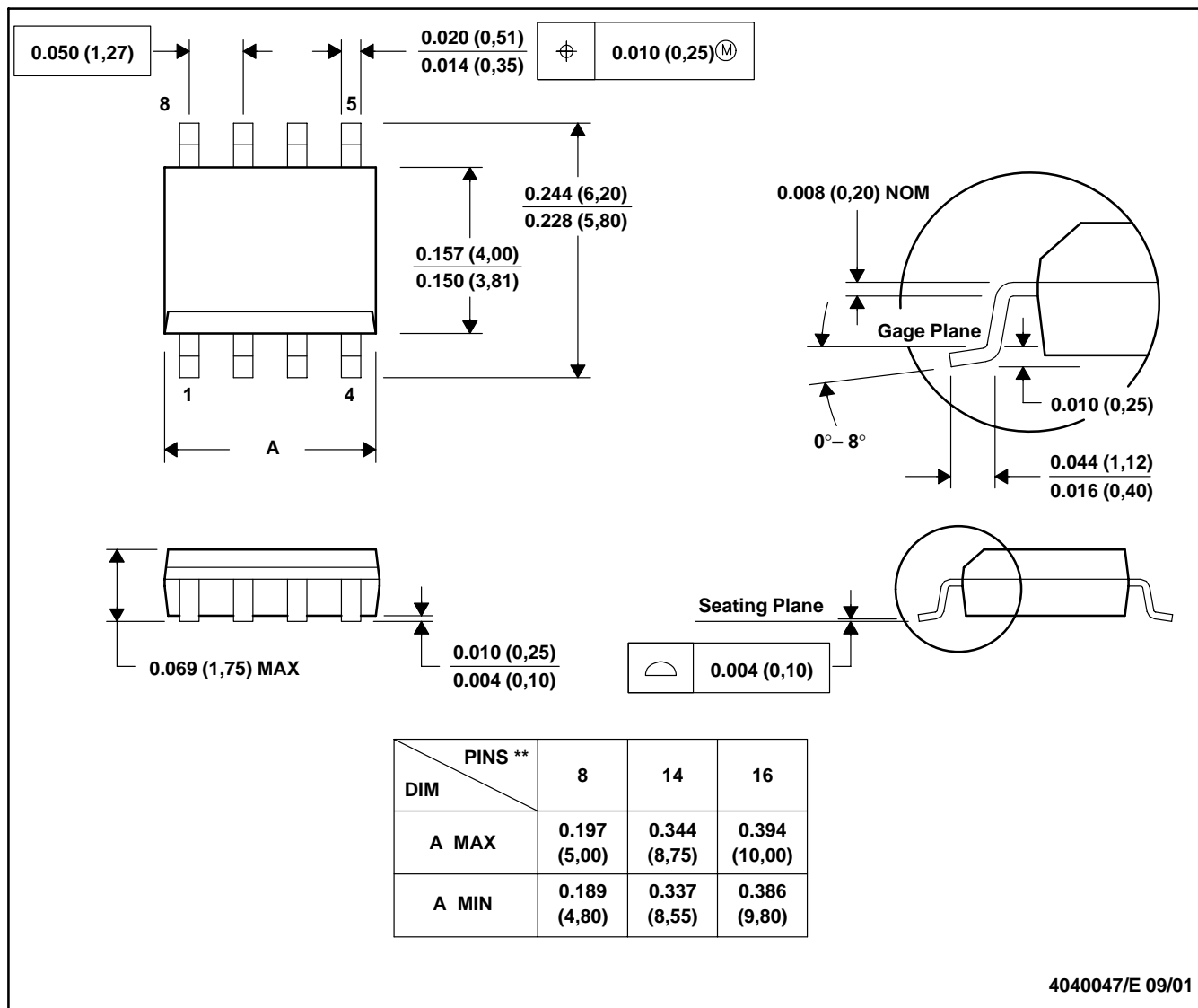


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN

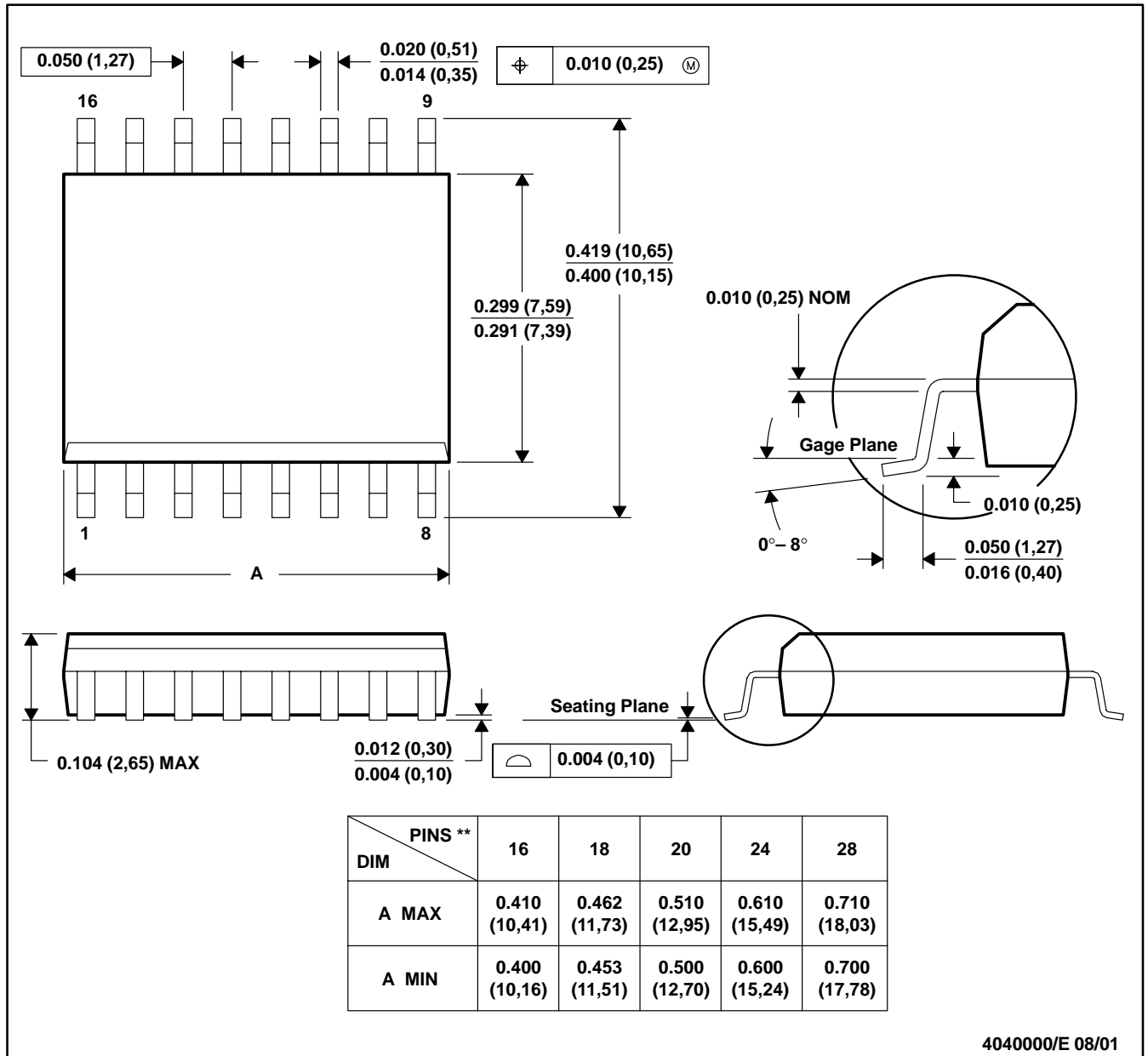


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



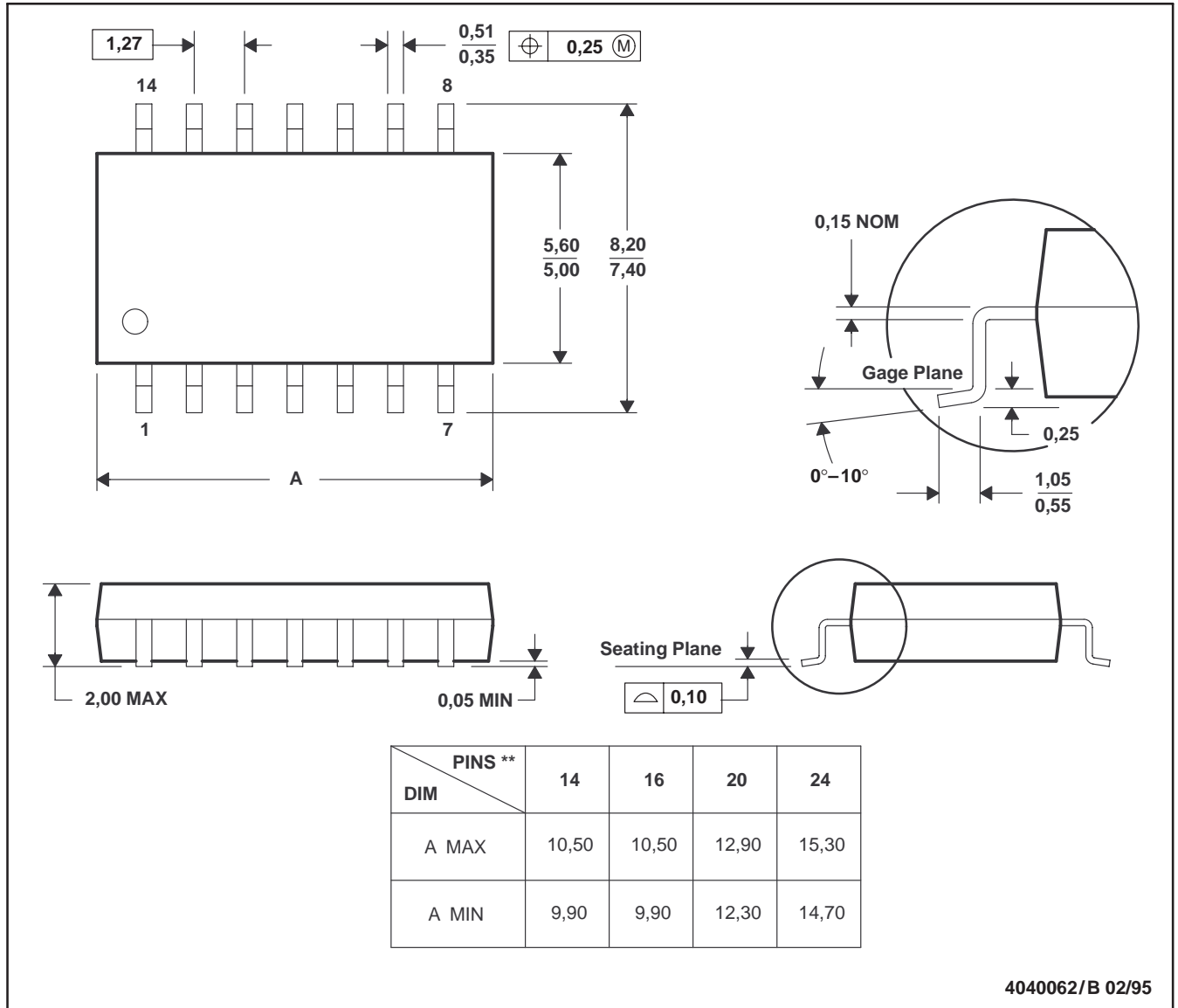
4040000/E 08/01

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265