Futaba

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蛍光表示管製品規格
VACUUM FLUORESCENT DISPLAY SPECIFICATION

双葉電子工業株式会社
電子部品事業部　電子管技術グループ
ENGINEERING GROUP, ELECTRON TUBE
ELECTRONIC COMPONENTS DIVISION
FUTABA CORPORATION

形名 Type No.　16-SD-13GINK

用　途 :Application　STB
外形寸法 :Outer Dimension　100.0 (L) × 16.2 (W) × 6.1 (T)mm
Cadmium Free Phosphor, Lead Free Solder
発光色 :Color of Illumination Green (G. x=0.24,y=0.41)

絶対最大定格:Absolute Maximum Rating

項目 : Item		Symbol	Terminals	Rating	Unit
フィラメント電圧 :Filament Voltage	*1	Ef	F1-F2	5.0	Vac
ロジック電源電圧 :Logic Supply Voltage	*3,*4	V_{DD}	V_{DD}	−0.3 ～ 6.0	Vdc
ドライバ電源電圧 :Driver Supply Voltage	*3	V_H	V_H	−0.3 ～ 43	Vdc
ロジック信号入力電圧 :Logic Input Voltage		V_{IN}	SI,CLK,LAT,BK	−0.3 ～ V_{DD}+0.3	Vdc
保存温度 :Storage Temperature		T_{stg}	−	-55 ～ +80	℃

絶対最大定格:瞬時たりとも超えてはならない規格であり、此れを超えた場合恒久的な機能障害を発生する可能性があります。
Absolute Maximum Condition : The value shall not be exceeded in any conditions. Permanent damage to VFD may be expected.

推奨動作条件:Recommended Operating Condition

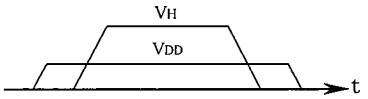
項目 : Item		Symbol	Min.	Typ.	Max.	Unit
フィラメント電圧 :Filament Voltage	*1	Ef	3.78	4.2	4.62	Vac
ドライバ電源電圧 :Driver Supply Voltage	*3	V_H	32	36	40	Vdc
ロジック電源電圧 :Logic Supply Voltage	*3	V_{DD}	4.5	5.0	5.5	Vdc
Hレベル入力電圧 :H-Level Input Voltage		V_{IH}	V_{DD}×0.8	−	V_{DD}	Vdc
Lレベル入力電圧 :L-Level Input Voltage		V_{IL}	0	−	V_{DD}×0.2	Vdc
カットオフバイアス :Cut-off Bias	*2	Ek	5.0	−	7.5	Vdc
動作温度 :Operating Temperature		T_{opr}	-20	−	+70	℃

内部クロック動作特性:Characteristics of Internal Clock Circuit

項目 : Item	Symbol	条件:Condition	Typ.	Unit
自己発信周波数 :Internal Clock Frequency	f_{OSC}	V_{DD}=5.0V R_{OSC}=16kΩ	2.4	MHz
表示フレーム周波数 :Display Frame Frequency	f_{FR}		586	Hz

推奨動作条件:信頼性、品質を確保できうる範囲(寿命はTyp.値が最適値です。)
Recommended Operating Condition:Quality and reliability can be assured in this condition.
(Typ.condition is the most optimized value on the life time.)

*1 AC50、60Hzまたは30kHz以上の実効値。50Hz,60Hz or > 30kHz r.m.s.
*2 フィラメントトランスのセンタータップに印加する。Ek is applied to the center tap of the filament transformer.
*3 電源シーケンス　Power Supply Sequence
VHを印加中はVDDを4.5～5.5Vの間でご使用下さい。
VDD should be 4.5 to 5.5V when applying VH.
電源投入時はV_{DD}とV_Hを同時、またはV_{DD}を投入した後にV_Hを投入下さい。
V_H and V_{DD} should be on at the same,or V_H should be on after V_{DD} is on.
電源遮断時はV_{DD}とV_Hを同時、またはV_Hを遮断した後にV_{DD}を遮断下さい。
V_H and V_{DD} should be off at the same,or V_{DD} should be off after V_H is off.



電源シーケンス
Power Supply Sequence

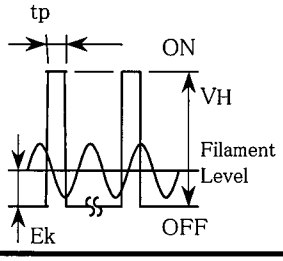
*4 V_Hを印加中は推奨動作条件でご使用下さい。Recommended Operating Condition should be used when applying VH.

本製品は半導体製品ですので静電気のお取り扱いには十分ご注意お願いします。
The VFD is built with C-MOS Ics.Precautions should be taken to minimize the possibility of static charges.
本規格と異なる使い方をされる場合、品質,信頼性を確保出来ない場合がありますので事前にご相談下さい。
Since deviation from this specification may generate quality or reliability concerns, please consult to FUTABA prior to use.
この仕様書の内容はお断りなく変更することがありますのでご了承下さい。
This specification is subject to change without notice.

電気的特性:Electrical Characteristics

指定がない場合は、推奨動作条件のTyp値、全点灯、f_{CLK}=0.5MHz、PGND=LGND=0Vとする。

Unless otherwise specified, The test condition should be Typ value of recommended condition and all segments on, f_{CLK}=0.5MHz,PGND=LGND=0V.

項目 : Item	Test Condition	Symbol	Min.	Typ.	Max.	Unit.
フィラメント電流 Filament Current	Ef = 4.2 Vac V_H=V_{DD}=0V	If	50	55	61	mAac
ロジック電源電流 Logic Supply Current	全点灯 All Segments on	I_{DD}	—	-	5.0	mA
ドライバ電源電流 Driver Supply Current	全点灯 All Segments on	$I_{H(AVG)}$	—	5.0	10	mA
	全点灯 All Segments on	$I_{H(PEAK)}$ timming T1,16	—	6.0	12	mA
Hレベル入力電流 H-Level Input Current	V_{IN}=V_{DD} $\overline{CS}$,DA,CP, $\overline{RESET}$	I_{IH}	—	—	5	μA
Lレベル入力電流 L-Level Input Current	V_{IN}=0V $\overline{CS}$,DA,CP, $\overline{RESET}$	I_{IL}	—	—	-5	μA
輝 度 Luminance	Ef = 4.2 Vac V_{DD} = 5.0 Vdc V_H = 36 Vdc *(Ek = 5.0) Dimming = 240/255 (Duty =1/17)  	L(G.)	440	880	-	cd/m^2
		L( )			-	cd/m^2
		L( )			-	cd/m^2
		L( )			—	cd/m^2
		L( )			—	cd/m^2
		L( )			—	cd/m^2
輝度比 Luminance Ratio between Digits		$\frac{Lmax}{Lmin}$	—	—	2	

*( ) 内は, センタータップを接地した場合である.

The value in *( ) is shown for the center tap grounded.

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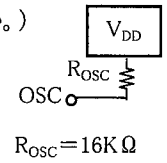
●機能表:Function Table

機能 Function	記号 Symbol	入力／出力 Input／Output	内容 Description
シフトクロック入力端子 Shift Clock Input	CP	入力 Input	CPの立ち上がりでシリアルデータがシフトします。 Serial data is shifted on the rising edge of CP
シリアルデータ入力 Serial Data Input	DA	入力 Input	LSB側より入力します。 Input from LSB.
テスト端子 A Test Pin A	TSA	–	オープンにして下さい。 Leave this open. This is for factory use.
テスト端子 B Test Pin B	TSB	–	L-GNDに接続して下さい。 Connect it with L-GND.
チップセレクト入力端子 Chip Select Input	$\overline{CS}$	入力 Input	$\overline{CS}$をハイレベルにするとデータのシリアル転送が禁止されます。 Serial data transfer is disabled when CS pin is "H" level.
リセット入力端子 Reset Input	$\overline{RESET}$	入力 Input	$\overline{RESET}$をローレベルにすると全ての機能を初期化します。 "Low" initializes all the functions. 初期状態リセット機能を参照して下さい。 For an initial status, see Reset Function
自己発振用端子 Pin for self-oscillation.	OSC	入力/出力 Input/Output	自己発振用端子です。 (外部からクロックを与えて使用しないで下さい。) Pin for self-oscillation. (Do not apply external clocks to these pins) 抵抗を接続します。 Connect this pin to resisitor.  R_{OSC}=16KΩ
ロジック電源端子 Logic Supply Pin	VDD	入力 Output	ロジック回路のための電源端子 Power Supply pin for Logic Circuit
ドライバ電源端子 Driver Supply Pin	VH	入力 Input	ドライバのための電源端子 Power Supply pin for Driver Output
ロジックグランド端子 Logic GND Pin	LGND	入力 Input	ロジックのグランド GND for Logic Circuit
パワーグランド端子 Power GND Pin	PGND	入力 Input	VHのグランド GND for VH Circuit
フィラメント端子 Filament Pin	F1,F2	入力 Input	フィラメント電圧入力端子 Filament Voltage input
ノーピン No Pin	NP	–	NP部にはピンはありません。 There is no pin.
ノーエクステンド No Extend Pin	NX	–	ノーコネクションのピンです。 There is no connection.

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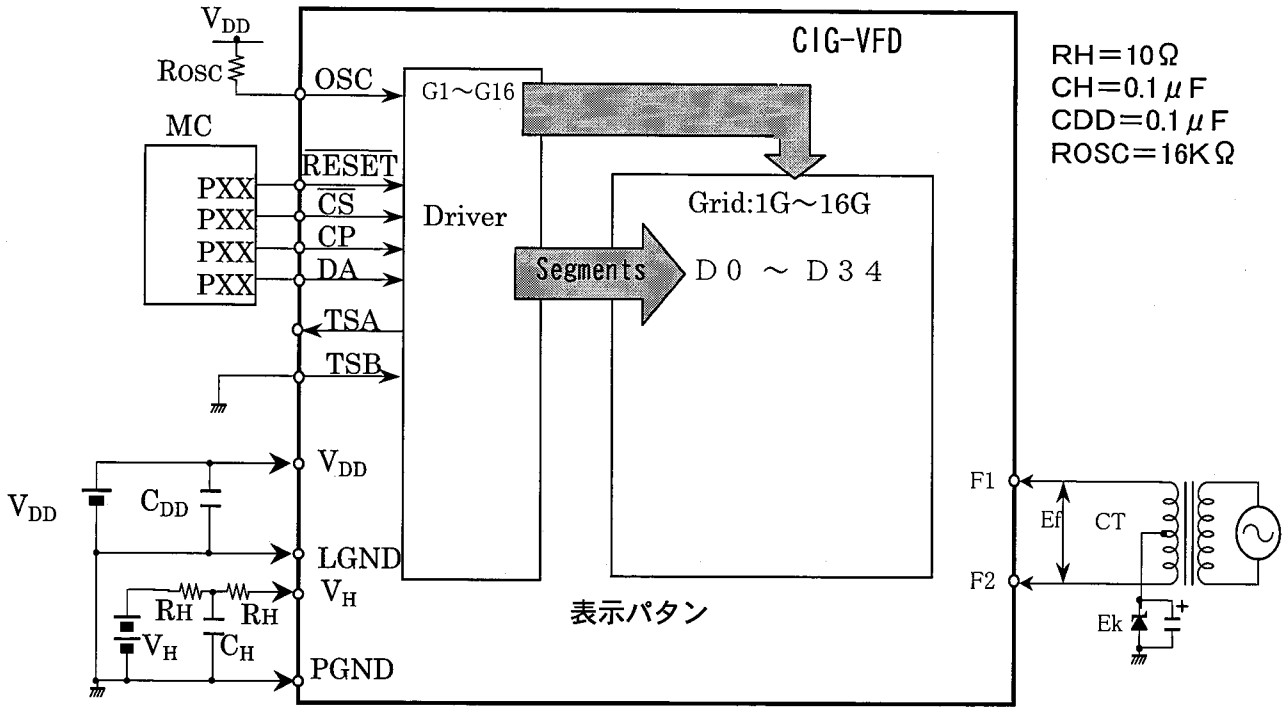
接続回路(例)



注1)直流抵抗RHは電流制限用の抵抗です。CH,CDDはノイズフィルター用のパスコンです。

Note1)The series resister RH is resister for limitation of over current.CH and CDD is the capacitors for noise filter to the VH and VDD.

注2)本製品はICを含むデバイスです。ICの破壊モード(ショートモード)に対応する回路設計を推奨します。

Note2)This product is the device with built－in IC. The design of the PWB should be considered for the destructive mode (short mode) of IC.

● Timing condition

The timing condition for serial transfer is shown below.

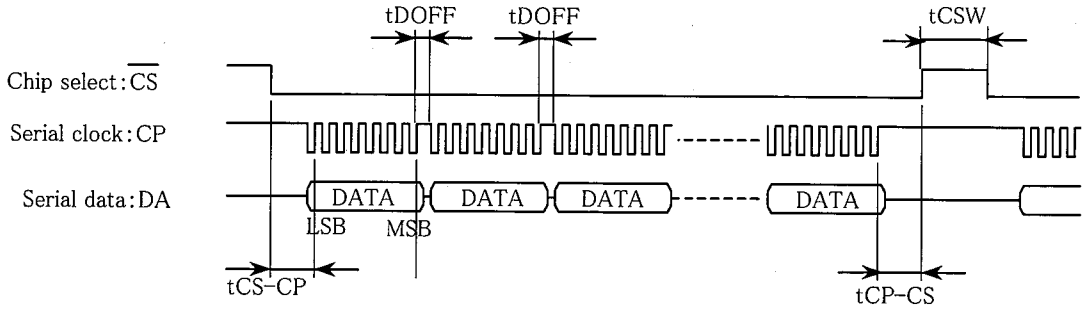


Fig. 2-2-1 Timing Condition of Serial Data Transfer

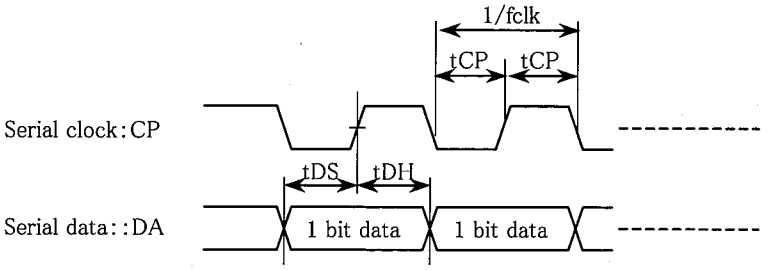


Fig. 2-2-2 Timing Condition of Serial Clock

Table 2-1 Timing Condition

Item	Symbol	Condition	Min	Typ	Max	Unit
CP frequency	fclk	-	-	-	0.5	MHz
CP pulse width	tCPW	-	(700)	-	-	ns
Time needed between CS and CP	tCS-CP	-	(1000)	-	-	ns
Time needed between CP and CS	tCP-CS	-	(1000)	-	-	ns
Time to wait CS	tCSW	oscillating	(1000)	-	-	ns
Time to process data	tDOFF	oscillating	(2000)	-	-	ns
Time to set up data	tDS	-	(300)	-	-	ns
Time to hold data	tDH	-	(300)	-	-	ns

● Commands

1. List of commands.

Table 1 shows the list of commands.

Table 1 Commands

Command	MSB 1st Byte							LSB	MSB 2nd Byte							LSB	
	B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0	
DCRAM_A DATA WRITE	0	0	1	X4	X3	X2	X1	X0	C7	C6	C5	C4	C3	C2	C1	C0	
CGRAMDATA WRITE	0	1	0	*	*	Y2	Y1	Y0	*	D30	D25	D20	D15	D10	D5	D0	2nd Byte
									*	D31	D26	D21	D16	D11	D6	D1	3rd Byte
									*	D32	D27	D22	D17	D12	D7	D2	4th Byte
									*	D33	D28	D23	D18	D13	D8	D3	5th Byte
									*	D34	D29	D24	D19	D14	D9	D4	6th Byte
ADRAM DATA WRITE	0	1	1	X4	X3	X2	X1	X0	*	*	*	*	E3	E2	E1	E0	
URAM DATA WRITE	1	0	0	*	*	U2	U1	U0	8G	7G	6G	5G	4G	3G	2G	1G	
									16G	15G	14G	13G	12G	11G	10G	9G	
DIGIT SET OF DISPLAY TIMING	1	1	1	0	0	0	*	*	UV	F6	F5	F4	F3	F2	F1	F0	
DIMMING SET	1	1	1	0	0	1	*	*	H7	H6	H5	H4	H3	H2	H1	H0	
DISPLAY LIGHT ON/OFF	1	1	1	0	1	0	LS	HS	*	*	*	*	*	*	*	*	
STAND-BY MODE SET	1	1	1	0	1	1	*	ST	*	*	*	*	*	*	*	*	

Notes:

*=Not Relevant.

Xn=Duty Timing (Digit) Address Set, n=0 to 4.

Cn=CGRAM/CGROM Character Code Bit, n=0 to 7.

Yn=CGRAM Address Bit, n=0 to 2.

Dn=CGRAM Character Code Setting, n=0 to 34.

En=Segment Pin Setting, n=0 to 3.

Un=URAM Address Set, n=0 to 2.

Gn=Grid ON/OFF Setting, n=1 to 16.

Fn=Number of Digits Set, n=0 to 6.

UV="1": Universal Function Enable. UV="0": Universal Function Disable.

Hn=Dimming Quantity Setting, n=0 to 7.

HS="1": All Output (Anode, Segment) Data="H". HS="0": Normal Mode.

LS="1": All Output (Anode, Segment) Data="L". LS="0": Normal Mode.

ST="1": Stand-by Mode. ST="0": Normal Mode.

In case of continuous data write-in to RAM (DCRAM, CGRAM, ADRAM, URAM, etc.), it is not necessary to specify the first byte of the second and later bytes, because the addresses are automatically incremented internally.

Note : There is no guarantee for any operation resulted from the setting using other commands listed above.

※ The type isn't used in all lights ON.

2 Description of commands

2.1 DCRAM data write command

The DCRAM (data control RAM) has a 5-bit address to store the character codes of the CGROM and the CGRAM. The character codes specified by the DCRAM are converted into the character pattern of 5x7 dot matrix via the CGROM or the CGRAM.

To write-in the DCRAM, specify the DCRAM address and write-in the character codes of the CGROM and the CGRAM. For the setting relationship of the DCRAM address to the display timing, refer to section 2.4, Display timing set command. The command format is shown below.

【Command Format】

	MSB							LSB	
	B7	B6	B5	B4	B3	B2	B1	B0	
1st byte (1st)	0	0	1	X4	X3	X2	X1	X0	The DCRAM data write mode is selected and the DCRAM address is specified. (Ex. The DCRAM address 0H is specified.)
2nd byte (2nd)	C7	C6	C5	C4	C3	C2	C1	C0	The CGROM and CGRAM character codes are specified. (The specified character codes are written into the DCRAM address 00H.)

●To continuously specify the CGROM and CGRAM character codes, specify character codes only as shown below. As the DCRAM addresses are automatically incremented, it is not necessary to specify the first byte. Addresses are specified from 00H to 17H incrementing 1 by 1. It is possible to continuously transfer up to 24 addresses.

	MSB							LSB	
	B7	B6	B5	B4	B3	B2	B1	B0	
3rd byte (3rd)	C7	C6	C5	C4	C3	C2	C1	C0	The CGROM and CGRAM character codes are specified. (The data are written into the DCRAM address 01H.)
4th byte (4th)	C7	C6	C5	C4	C3	C2	C1	C0	The CGROM and CGRAM character codes are specified. (The data are written into the DCRAM address 02H.)
⋮									
25th byte (25th)	C7	C6	C5	C4	C3	C2	C1	C0	The CGROM and CGRAM character codes are specified. (The data are written into the DCRAM address 17H.)
26th byte (26th)	C7	C6	C5	C4	C3	C2	C1	C0	The CGROM and CGRAM character codes are specified. (The data are written into the DCRAM address 00H.)

X0(LSB)～X4(MSB) : DCRAM address (5 bits: 24 characters)
C0(LSB)～C7(MSB) : CGROM and CGRAM codes (8 bits: 256 characters)

2.2 CGRAM data write command

The CGRAM (character generator RAM) has a 3-bit address to store character Patterns of 5x7 dot matrix. Character patterns stored in the CGRAM can be outputted by specifying the character code (address) of DCRAM. The CGRAM addresses are assigned from 00H to 07H. (The other addresses are all for CGROM.) The CGRAM can store 8 types of character pattern.

The CGRAM can be written-in by specifying its address.
The command format is shown below.

【Command Format】

	MSB							LSB	
	B7	B6	B5	B4	B3	B2	B1	B0	
1st byte (1st)	0	1	0	*	*	Y2	Y1	Y0	The CGRAM data write command and the CGRAM address are specified. (Ex: The CGRAM address 00H is specified.)
2nd byte (2nd)	*	D30	D25	D20	D15	D10	D5	D0	The data in the first row is specified. (The data is written into the CGRAM address 00H.)
3rd byte (3rd)	*	D31	D26	D21	D16	D11	D6	D1	The data in the second row is specified. (The data is written into the CGRAM address 00H.)
4th byte (4th)	*	D32	D27	D22	D17	D12	D7	D2	The data in the third row is specified. (The data is written into the CGRAM address 00H.)
5th byte (5th)	*	D33	D28	D23	D18	D13	D8	D3	The data in the fourth row is specified. (The data is written into the CGRAM address 00H.)
6th byte (6th)	*	D34	D29	D24	D19	D14	D9	D4	The data in the fifth row is specified. (The data is written into the CGRAM address 00H.)

●To continuously specify character pattern data, specify the character pattern data only as shown below. As the DCRAM addresses are automatically incremented, it is not necessary to specify the first byte. The character pattern data of the 2nd to the 6th byte are considered as one data. The time between bytes t_{DOFF} is 2us(min).

	MSB							LSB	
	B7	B6	B5	B4	B3	B2	B1	B0	
7nd byte (7th)	*	D30	D25	D20	D15	D10	D5	D0	The data in the first row is specified. (Written into the CGRAM address 01H.)
11th byte (11th)	*	D34	D29	D24	D19	D14	D9	D4	The data in the fifth row is specified. (Written into the CGRAM address 01H.)

Y0(LSB)～Y2(MSB) : CGRAM address (3 bits: for 8 characters)
D0(LSB)～D34(MSB): character pattern data (35 bits: 35 outputs for a digit)
*: Don't Care

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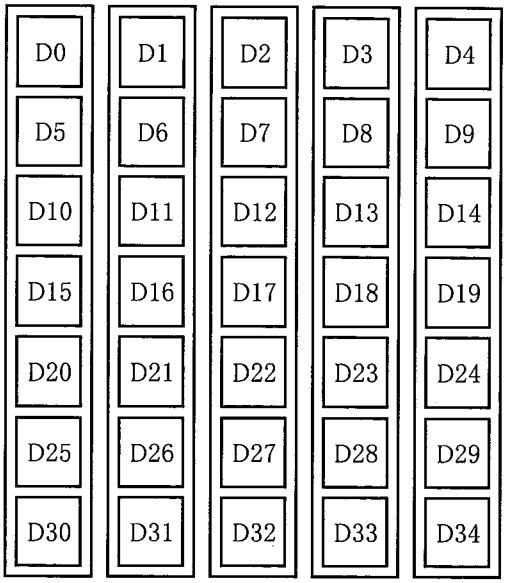
【Setting relationship of CGRAM Addresses】

HEX	Y2	Y1	Y0	Specified CGRAM
0	0	0	0	RAM00 (00H)
1	0	0	1	RAM01 (01H)
2	0	1	0	RAM02 (02H)
3	0	1	1	RAM03 (03H)
4	1	0	0	RAM04 (04H)
5	1	0	1	RAM05 (05H)
6	1	1	0	RAM06 (06H)
7	1	1	1	RAM07 (07H)

【Setting relationship CGRAM Outputs】



・The setting relationship of CGRAM outputs may vary depending on the VFD product.

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2.3 ADRAM data write command

The ADRAM (Additional Data RAM) has a 5-bit address to store data.
The signal data specified by the ADRAM is directly outputted. The ADRAM stores up to 4 output patterns (AD1 to AD4) for each digit.
To write the ADRAM data, specify the ADRAM address before writing-in data.
Please refer to the Page8 anode connection for the position of set ADRAM address and display timing.
The command format is shown below.

【Command Format】

	MSB B7	B6	B5	B4	B3	B2	B1	LSB B0	
1st byte (1st)	0	1	1	X4	X3	X2	X1	X0	To select the ADRAM data write and to specify the ADRAM address. (Ex: To specify the ADRAM address 00H.)
2nd byte (2nd)	*	*	*	*	E3	E2	E1	E0	To specify the signal data. (Ex: To write-in the data to the ADRAM address 00H.)

●To continuously specify the signal data, specify the character codes only as shown below.
Since the ADRAM addresses are automatically incremented, it is not necessary to specify the 1st byte.
Addresses are specified from 00H to 17H incrementing 1 by 1.

	MSB B7	B6	B5	B4	B3	B2	B1	LSB B0	
3rd byte (3rd)	*	*	*	*	E3	E2	E1	E0	To specify the signal data. (The data is written into the ADRAM address 01H.)
4th byte (4th)	*	*	*	*	E3	E2	E1	E0	To specify the signal data. (The data is written into the ADRAM address 02H.)
⋮									
25th byte (25th)	*	*	*	*	E3	E2	E1	E0	To specify the signal data. (The data is written into the ADRAM address 17H.)
26th byte (26th)	*	*	*	*	E3	E2	E1	E0	To specify the signal data. (The data is written into the ADRAM address 00H.)

X0(LSB)～X4(MSB) : ADRAM address (5-bit)
E0(LSB)～E3(MSB) : AD1～AD4 output data
0: output OFF 1: output ON
* : Don't Care

2.4 Display timing set command

The display timing command sets the display timing including the universal timing using 8-bit data. When the power is supplied or the RESET signal is inputted, the value is set to the initial value (1G to 16G). Be sure to execute this command before turning on the display light. Then, set the fixed value for each VFD. For the set value, refer to the individual VFD specification. The command format is shown below.

【Command Format】

	MSB							LSB	
	B7	B6	B5	B4	B3	B2	B1	B0	
1st byte (1st)	1	1	1	0	0	0	*	*	To select the display timing set.

	MSB							LSB	
	B7	B6	B5	B4	B3	B2	B1	B0	
2nd byte (2nd)	UV	F6	F5	F4	F3	F2	F1	F0	To select the display timing set and the universal timing enable/disable.

	Set data (F3~F0)				Set timing (Grid output used)
	F3	F2	F1	F0	
	0	0	0	0	T1(1G)
	0	0	0	1	T1(1G)~T2(2G)
	0	0	1	0	T1(1G)~T3(3G)
	0	0	1	1	T1(1G)~T4(4G)
	0	1	0	0	T1(1G)~T5(5G)
	0	1	0	1	T1(1G)~T6(6G)
	0	1	1	0	T1(1G)~T7(7G)
	0	1	1	1	T1(1G)~T8(8G)
	1	0	0	0	T1(1G)~T9(9G)
	1	0	0	1	T1(1G)~T10(10G)
	1	0	1	0	T1(1G)~T11(11G)
	1	0	1	1	T1 (1G)~T12(12G)
	1	1	0	0	T1(1G)~T13(13G)
	1	1	0	1	T1(1G)~T14(14G)
	1	1	1	0	T1(1G)~T15(15G)
☆	1	1	1	1	T1(1G)~T16(16G)

	Set data (UV,F6~F4)				Set timing (Grid output used)
	UV	F6	F5	F4	
☆	0	*	*	*	Universal display timing (T17~T24) is not used.
	1	0	0	0	T17 (Grid output follows the URAM setting.)
	1	0	0	1	T17~T18 (Grid output follows the URAM setting.)
	1	0	1	0	T17~T19 (Grid output follows the URAM setting.)
	1	0	1	1	T17~T20 (Grid output follows the URAM setting.)
	1	1	0	0	T17~T21 (Grid output follows the URAM setting.)
	1	1	0	1	T17~T22 (Grid output follows the URAM setting.)
	1	1	1	0	T17~T23 (Grid output follows the URAM setting.)
	1	1	1	1	T17~T24 (Grid output follows the URAM setting.)

*: Don't Care

☆The command of 16-SD-13GINK as below.

UV	F6	F5	F4	F3	F2	F1	F0
0	*	*	*	1	1	1	1

2.5 URAM control set command

The URAM (Universal Data RAM) has a 3-bit address to store the grid output data in the universal timing mode. The output data specified by the URAM is directly outputted in the universal mode. The URAM stores the output pattern of 16 grids for each timming. For the setting to the URAM, refer to the individual VFD specification, because setting values are fixed for each VFD. To write the URAM, specify the RAM address frist, then write-in the grid output data. The command format is shown below.

【Command Format】

	MSB							LSB	
	B7	B6	B5	B4	B3	B2	B1	B0	
1st byte (1st)	1	0	0	*	*	U2	U1	U0	To select the URAM data write-in and the UDRAM address. (Ex: The URAM address 00H is specified.)

	MSB							LSB	
	B7	B6	B5	B4	B3	B2	B1	B0	
2nd byte (2nd)	8G	7G	6G	5G	4G	3G	2G	1G	To write-in the grid output data of 1G to 8G. (The data is written-into the URAM address 00H.)

	MSB							LSB	
	B7	B6	B5	B4	B3	B2	B1	B0	
3rd byte (3rd)	16G	15G	14G	13G	12G	11G	10G	9G	To write-in the grid output data of 9G to 16G. (The data is written-into the URAM address 00H.)

●To continuously specify the output data, specify the grid output data only as shown below. As the URAM addresses are automatically incremented, it is not necessary to specify the first byte. The specified addresses are specified from 0H to 7H incrementing 1 by 1.
Time between bytes (t_{DOFF}) is 2us(min).

	MSB							LSB	
	B7	B6	B5	B4	B3	B2	B1	B0	
4th byte (4th)	8G	7G	6G	5G	4G	3G	2G	1G	To write-in the grid output data of 1G to 8G. (The data is written into the URAM address 01H.)

	MSB							LSB	
	B7	B6	B5	B4	B3	B2	B1	B0	
5th byte (5th)	16G	15G	14G	13G	12G	11G	10G	9G	To write-in the grid output data of 9G to 16G. (The data is written into the URAM address 01H.)

U0(LSB)～U2(MSB) : URAM address (3 bits)
1G～16G: grid output data 0: output OFF 1: output ON
* : Don't Care

●URAM address

Timing Name	URAM address			Remarks
	U2	U1	U0	
T17	0	0	0	Don't use
T18	0	0	1	Don't use
T19	0	1	0	Don't use
T20	0	1	1	Don't use
T21	1	0	0	Don't use
T22	1	0	1	Don't use
T23	1	1	0	Don't use
T24	1	1	1	Don't use

2.6 Dimming data write command

Brightness can be controlled in 240 levels using 8-bit data by setting the dimming data write command.
When the power is supplied or the RESET signal is inputted, the register value is set to 0.
Be sure to execute this command before turning on the display light. Then set the desired value.

【Command Format】

	MSB							LSB	
	B7	B6	B5	B4	B3	B2	B1	B0	
1st byte (1st)	1	1	1	0	0	1	*	*	To select the dimming data set.

	MSB							LSB	
	B7	B6	B5	B4	B3	B2	B1	B0	
2nd byte (2nd)	H7	H6	H5	H4	H3	H2	H1	H0	To select the dimming data set.

H0(LSB)～H7(MSB) : dimming data (8 bits: for 240 levels)
* : Don't Care

【Relationship between the dimming data and the dimming status】

H7	H6	H5	H4	H3	H2	H1	H0	Dimming data	Remarks
0	0	0	0	0	0	0	0	0/255	Initial value (*)
0	0	0	0	0	0	0	1	1/255	
0	0	0	0	0	0	1	0	2/255	
・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・	
1	1	1	0	1	1	1	1	239/255	
1	1	1	1	0	0	0	0	240/255	
1	1	1	1	0	0	0	1		
・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・		
1	1	1	1	1	1	1	1		

* The status when the power is supplied or the $\overline{\text{RESET}}$ signal is inputted.

2.7 Display light ON/OFF set command

The display light ON/OFF set command are used to turn on all the display lights or turn them off. The all display lights OFF mode is mainly used for blinking or protecting the display from any misoperation to be aused when the power is supplied.The command format is shown below.

【Command Format】

	MSB							LSB	
	B7	B6	B5	B4	B3	B2	B1	B0	
1st byte (1st)	1	1	1	0	1	0	LS	HS	To select the all display light ON/OFF and specify operation.

LS,HS: display operation data.
* : Don't Care.

●Set value and display status

LS	HS	Display status	Remarks
0	0	Normal operation	
1	0	All display lights OFF	* The status when the power is supplied or the RESET signal is inputted.
0	1	All display lights ON	Don't use it.
1	1	All display lights ON	Don't use it.

2.8 Stand-by mode command

The setting of the Stand-by mode command saves the power while the display is in the standing-by mode. The command format is shown below.

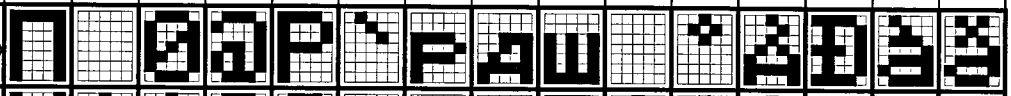
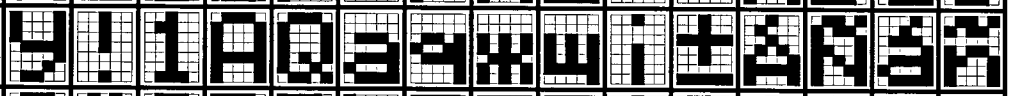
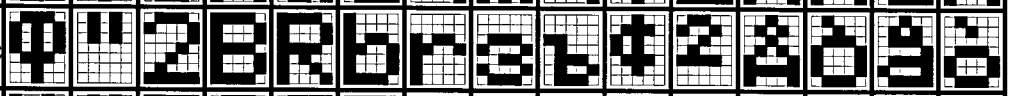
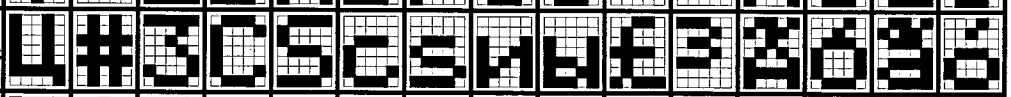
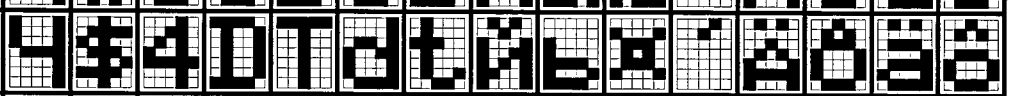
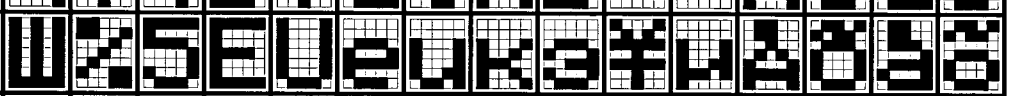
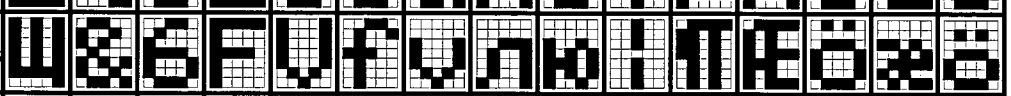
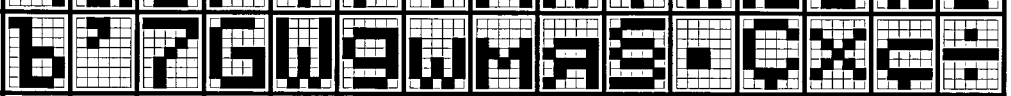
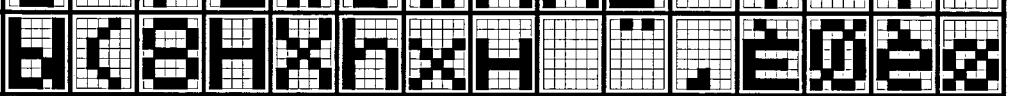
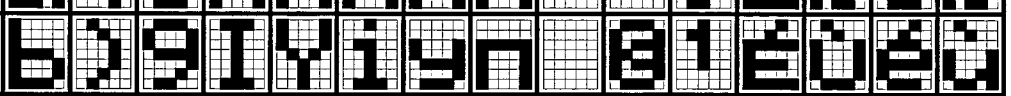
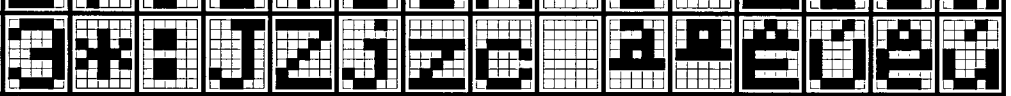
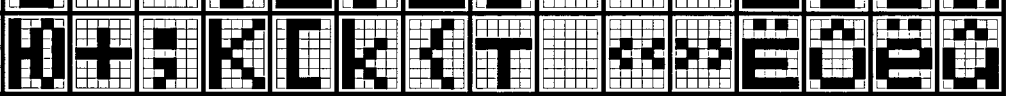
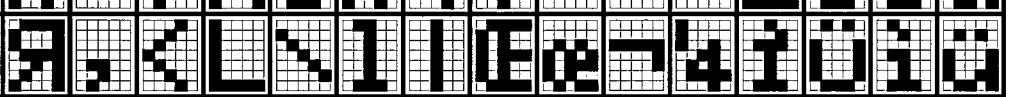
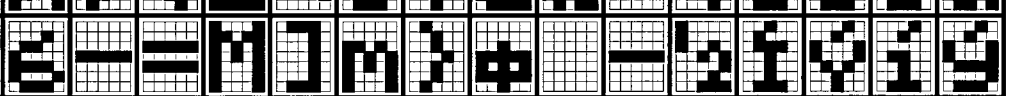
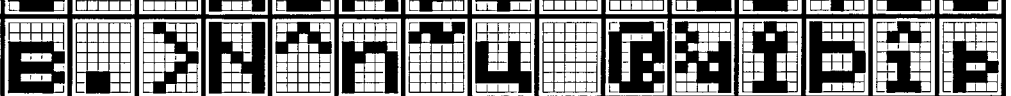
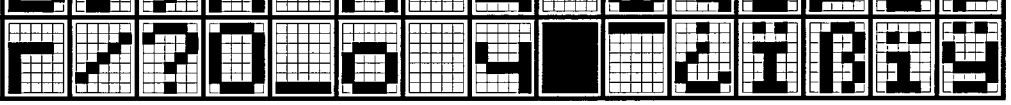
【Command format】

	MSB							LSB	
	B7	B6	B5	B4	B3	B2	B1	B0	
1st byte (1st)	1	1	1	0	1	1	*	ST	To select the stand-by mode and specify operation.

ST: Stand-by setting bit 0: normal operation mode, 1: stand-by mode.
*: Don't Care

2.8 CGROM codes

Table 2 CGROM Codes (General-purpose code : 07)

MSB / LSB	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	RAM0															
0001	RAM1															
0010	RAM2															
0011	RAM3															
0100	RAM4															
0101	RAM5															
0110	RAM6															
0111	RAM7															
1000																
1001																
1010																
1011																
1100																
1101																
1110																
1111																

* The addresses 00H to 07H are for the CGRAM address.

型名 Type No. 16-SD-13GINK

2.9 Initial value at the time reset

The initial value when the RESET signal is input is shown in Table 3.

Table 3 The initial value when the RESET signal is input

No.	Set to	Initial value
1	DCRAM	DCRAM Address=00H ALL DCRAM Data=20H
2	CGRAM	CGRAM Address=00H ALL CGRAM Data=00H
3	ADRAM	ADRAM Address=00H ALL ADRAM Data=00H Segment OFF (AD1～AD4 OFF)
4	URAM	URAM Disable URAM Address=00H ALL URAM Data=00H Grid OFF (1G～16G OFF)
5	Number of Digit Set	F3 ～ F0="1111"F6 ～ F4="000" UV="0" (Universal Function OFF)
6	Dimming Set	0/255
7	Display Light Set	LS="1" HS="0" (Display all off)
8	Stan-by Mode	ST="0" (Normal Mode)

● Flowchart of Commands

1 Basic flowchart of commands

The flowchart below shows the basic flow of commands from the time when power is turned on to the time when the display lights up. After the power is turned on, the values in 2 and 3 are set to the fixed value for each VFD used. Refer to the individual specification for the fixed value.

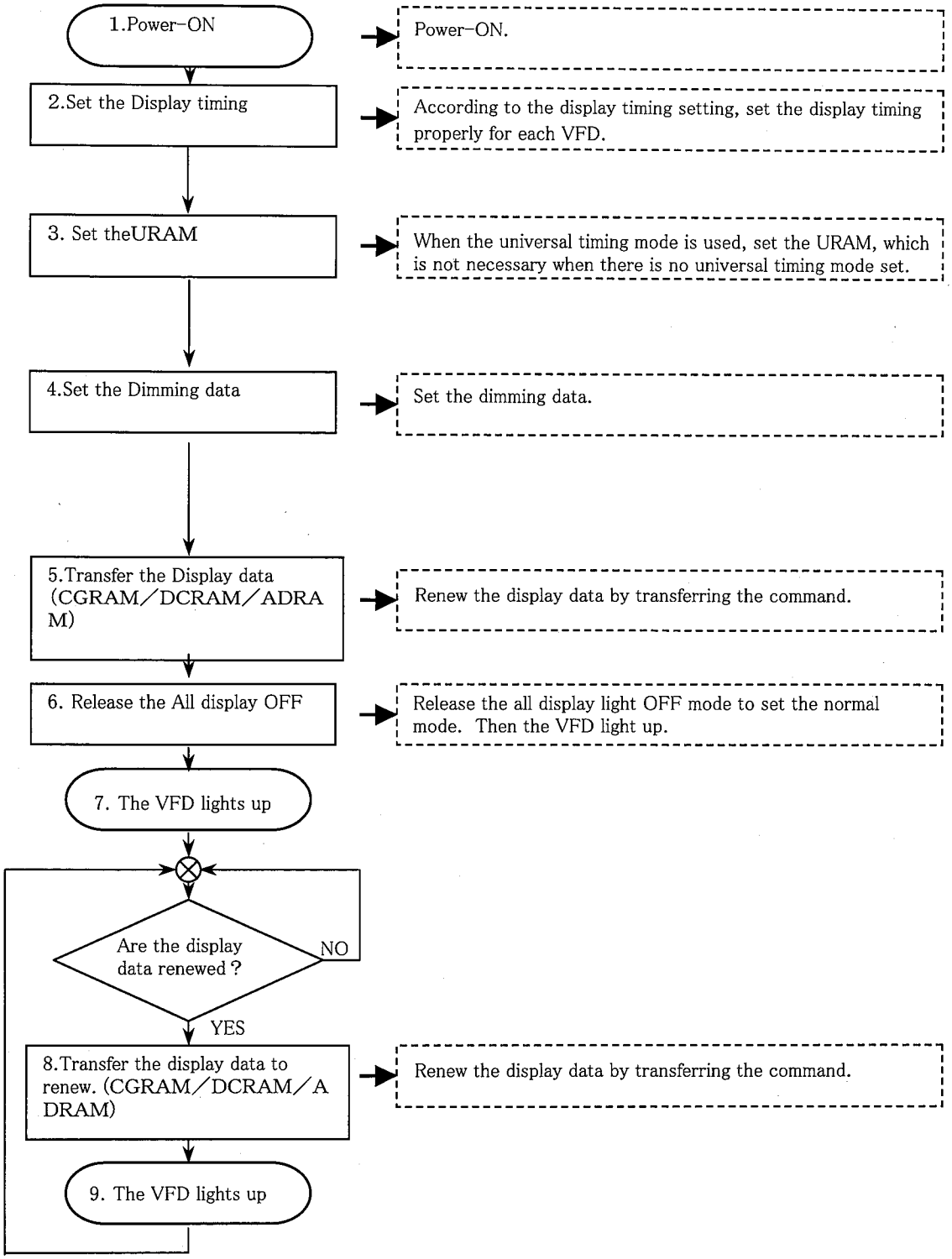


Fig. 4-1-1 Basic Command Flowchart

Note)For escaping error performance from noise,please regularly refresh and reset command entirely since initial set.

● Power-ON reset control

1 Power-ON reset circuit

For the power-on resetting, connect the resistor Rrst between the terminal to the logic power supply and the terminal to the system reset signal input, and the capacitor Crst between the RST terminal and the GND terminal。 An example of the circuit connection is shown below.

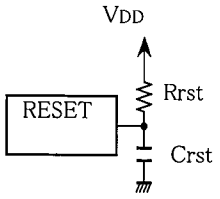


Fig.1 Power-ON reset circuit

2 Timing chart of resetting

Input the reset signal according to the figure shown below. Be sure not to transfer commands immediately after the reset signal is inputted. Because the command transferred before the definition of the internal status of the circuit may cause malfunction. Besides that, the value of tRST varies depending on the externally built parts. It is recommended to transfer the command after allowing sufficient time for the IC to be defined. For the initial value after resetting, refer to the section 2.9

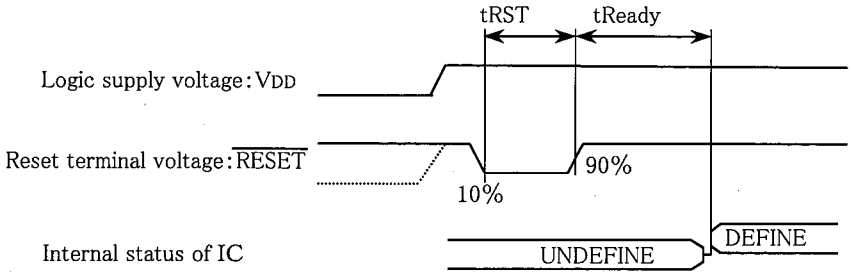


Fig. 2 Timing chart for resetting

Table 4 Time for Power-ON reset

項目 : Item	記号 SymAol	Min	Typ	Max	単位 Unit
リセットパルス時間 Reset Pulse Width	tRST	15	-	-	μs
リセット後ウエイト時間 Ready Time after Reset	tReady	2	-	-	ms

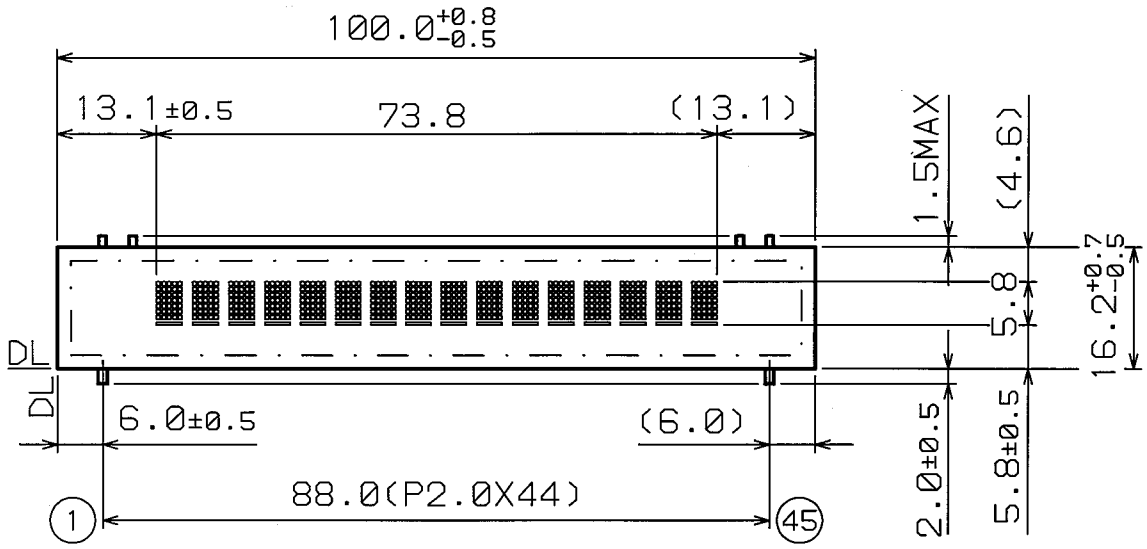
3. タイミングチャート ： Timing Chart

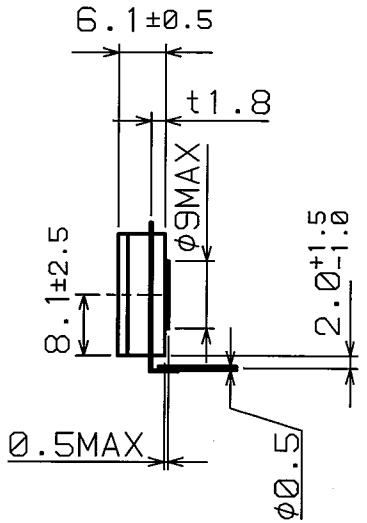
スキャンタイミング Grid Scan Timing	DCRAM／ ADRAM/GSRAM address	グリッドのオン／オフタイミング ON/OFF timing of Grid																Codes selection	
		1G	2G	3G	4G	5G	6G	7G	8G	9G	10G	11G	12G	13G	14G	15G	16G	DCRAM	ADRAM
T1	00H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	Note1	Note2
T2	01H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	Note1	Note2
T3	02H	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	Note1	Note2
T4	03H	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	Note1	Note2
T5	04H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	Note1	Note2
T6	05H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	Note1	Note2
T7	06H	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	Note1	Note2
T8	07H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	Note1	Note2
T9	08H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	Note1	Note2
T10	09H	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	Note1	Note2
T11	0AH	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	Note1	Note2
T12	0BH	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	Note1	Note2
T13	0CH	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	Note1	Note2
T14	0DH	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	Note1	Note2
T15	0EH	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	Note1	Note2
T16	0FH	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	Note1	Note2
T17	10H	Don't use it on this type.																*	*
T18	11H																	*	*
T19	12H																	*	*
T20	13H																	*	*
T21	14H																	*	*
T22	15H																	*	*
T23	16H																	*	*
T24	17H																	*	*

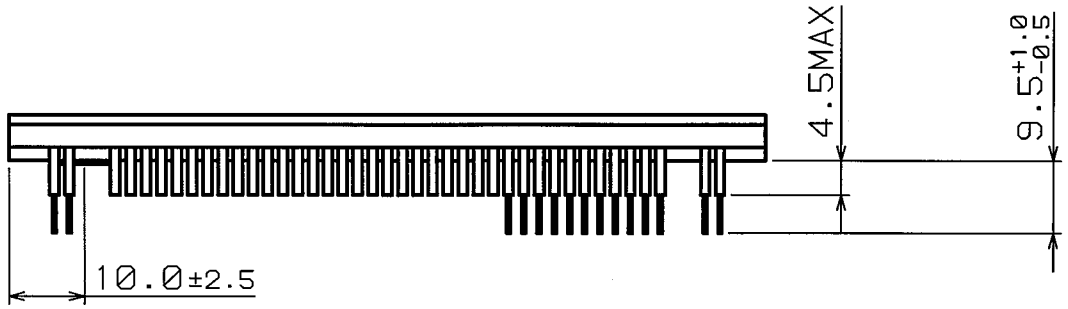
Note1 Set random code by CGROM code.

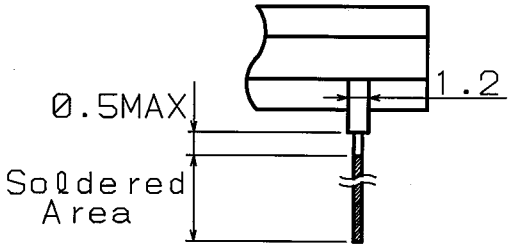
Note2 Set the standard pattern by CGRAM codes. Set CGRAM by P8.

*: Don't Care.









LEAD DETAILS

LEAD FREE SOLDER

(unit in mm)

16-SD-13GINK
OUTER DIMENSION

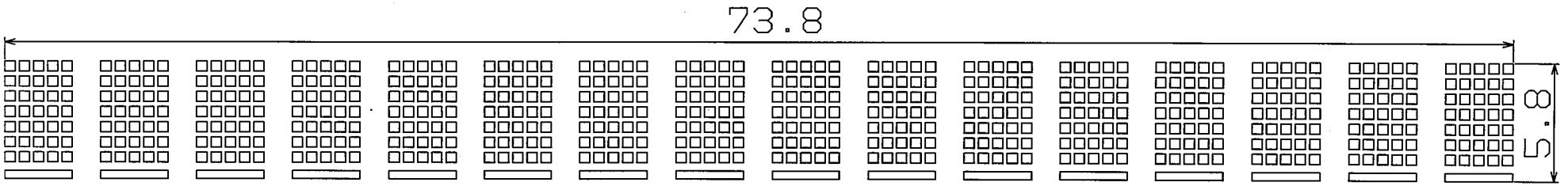
PIN CONNECTION

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45
CONNECTION	F1	F1	NP	NP	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	TSB	TSA	DA	CP	-CS	-RESET	OSC	VDD	VH	PGND	LGND	NP	NP	F2	F2

NOTE 1) F1,F2 --- Filament
2) NP ------ No pin
3) DL ------ Datum Line
4) NX ------ No extend pin
5) LGND ---- Logic GND pin
6) PGND ---- Power GND pin
7) VDD ----- Logic Voltage Supply pin
8) VH ------ High Voltage Supply pin
9) CP ------ Shift Register Clock
10) DA ------ Serial Data Input
11) $\overline{\text{TSA,B}}$ --- Test pin
12) $\overline{\text{CS}}$ ------ Chip Select Input pin
13) $\overline{\text{RESET}}$ --- Reset Input
14) OSC ----- Pin for self-oscillation
15) Solder composition is Sn-3Ag-0.5Cu.

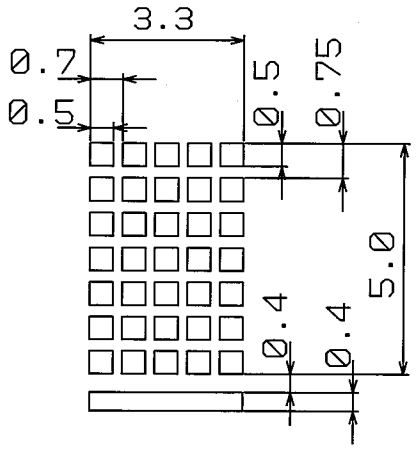
16-SD-13GINK
OUTER DIMENSION

PATTERN DETAIL



COLOR OF ILLUMINATION

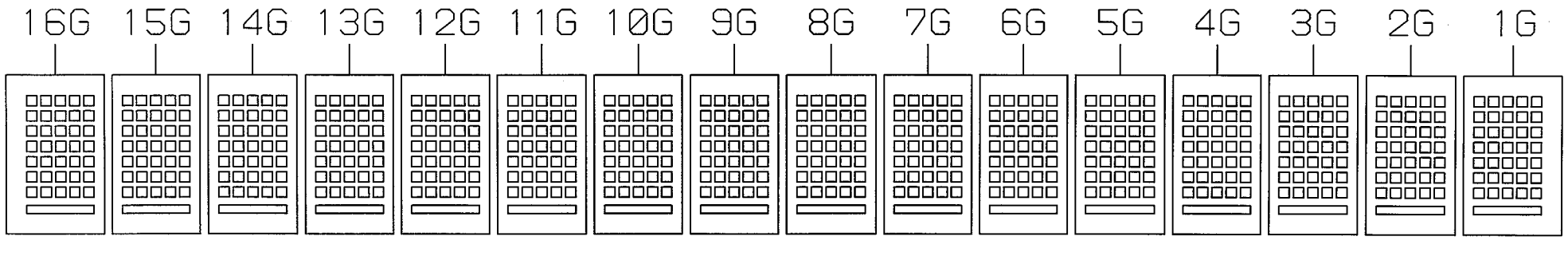
Green (G. x=0.24,y=0.41) - - - - - ALL graphics.

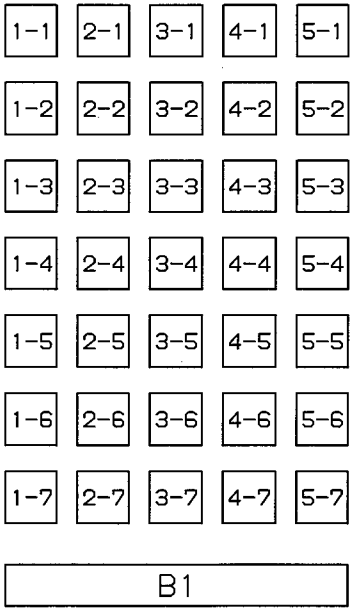


(unit in mm)

16-SD-13GINK
PATTERN DETAIL
COLOR OF ILLUMINATION

GRID ASSIGNMENT





(16G~1G)

16-SD-13GINK
GRID ASSIGNMENT

ANODE CONNECTION

	16G~1G
D0	1-1
D1	2-1
D2	3-1
D3	4-1
D4	5-1
D5	1-2
D6	2-2
D7	3-2
D8	4-2
D9	5-2
D10	1-3
D11	2-3
D12	3-3
D13	4-3
D14	5-3
D15	1-4
D16	2-4
D17	3-4
D18	4-4
D19	5-4
D20	1-5
D21	2-5
D22	3-5
D23	4-5
D24	5-5
D25	1-6
D26	2-6
D27	3-6
D28	4-6
D29	5-6
D30	1-7
D31	2-7
D32	3-7
D33	4-7
D34	5-7
AD1	B1

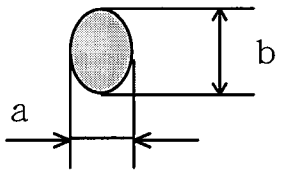
16-SD-13GINK
ANODE CONNECTION

Vacuum Fluorescent Display Quality Inspection Standard
蛍光表示管品質判定基準

General 一般

This standard should be adapted to the VFD quality inspection.
本仕様書は蛍光表示管の品質検査規格に適用される。

Inspection Condition 検査条件

Item	Condition
①VFD Operating Condition. VFD 駆動条件	Typ. Recommended Condition 推奨TYP. 駆動条件
②Inspection Aide 検査付帯条件	The inspection is to be performed with Futaba standard filter*1 or a applicable customer's filter and unaided eyes from 30cm distance under brightness of 90－110 lx. Futaba標準フィルター*1または顧客指定フィルターを通して30cmの距離から、90－110 lx の周囲照度にて、目視判定する。
③Defect Point Definition 不良点の測定方法	 $\phi S = \frac{a+b}{2}$

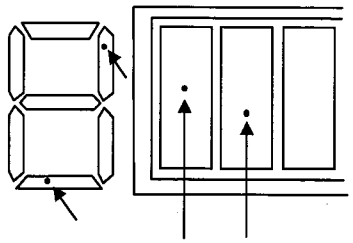
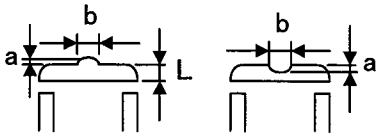
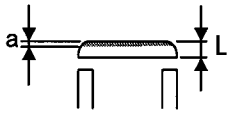
Limit sample should be provided upon mutual agreement by both parties when necessary.
限度見本は必要に応じ、両者協議の上設定するものとする。

Note *1
Futaba standard filter
双葉標準フィルター

Standard filter 標準フィルター	Type No. 型名	Manufacturer メーカー	Application 用途				
			Automotive 車載	Home Appliance 民生			
				Office machine 事務機	Consumer 家電用	Audio 音響	VTR
Gray smoke ｸﾞﾚｲｽﾓｰｸ	#530	MITSUBISHI RAYON 三菱レーヨン製	○	○	○		
Wine red ﾜｲﾝﾚｯﾄﾞ	PZ-1123-R	DIATEC ㈱ﾀﾞｲﾔﾃｯｸ製				○	○

形名 Type No.
16-SD-13GINK

Individual Quality Standard 個別品質基準

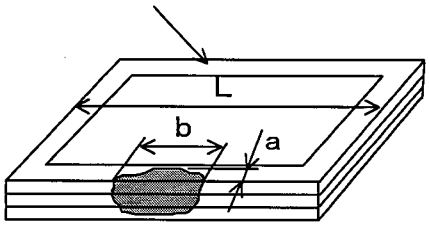
Item 項目	Phenomena 現象	Criterion 判定基準
①Foreign Particles・ Black Spot・ Printing Error 異物・黒点・ 印刷不良	Spots(Black spot)on the lighted segment due to dirt or dust. セグメントの斑点状の発光ムラ(黒点)。 	1.A black spot of over Φ0.3mm is counted as defected point. s=Φ0.3mmを超える物は不良とする。 2.In case of spot size is over Φ0.2mm,less than 0.3mm,one spot on the same segment, or maximum 3 spots in a display is to be allowed. Φ0.2mm以上Φ0.3mm以下は、セグメントに1箇まで、全セグメントに3箇所までを良品とする。 3.A spot of less than Φ0.2mm should not be counted as defect point. Φ0.2mm未満の物は個数に拘わらず良品とする。
②Irregularity of segment shape by printing error. ｾｸﾞﾒﾝﾄ凹凸・ 印刷不良	Partial irregularity on a segment. セグメント形状の部分的凹凸 	1.Acceptable size of irregularities with respect to the segment width(L). セグメント幅(L)に対する凹凸の許容寸法。 a=0.3mm max., b=0.3mm max.,acceptable. a=0.3mm 以下、b=0.3mm 以下を良品とする。 2.In case of the (L) below 0.5mm wide,the acceptable irregularities is a=1/2max. of the segment width(L). 尚、セグメント幅(L)が0.5mm以下の場合は、a≦1/2Lを良品とする。
③Uneven luminance 輝度ムラ	Partial dark area on the lighted segment. 発光面の部分的な輝度差	No significant irregularity of luminance is acceptable. 著しい物は無き事。
④Shaded Segment 字カケ	Shaded area appeared on the edge of segments セグメント端部の半影 	1.Shaded Segments up to 1/3 of the segment width are accepted. セグメント幅(L)の1/3までを良品とする。 2.In case of a segment below 0.5mm wide, the acceptable shaded segment should be up to 1/2 of the segment width. 但し、L≦0.5mmの場合は、1/2迄を良品とする。
⑤Extra lighting モレ発光	Undesirable lighting area or points, a star dust or a bright spot due like to extra phosphor particle. 発光パタン以外への蛍光体付着による星屑状、輝点状の不要発光	Extra lighting which can be clearly observed through the specified filter should be judged as a defect. 指定フィルターを通して不要発光のはっきり判る物を不良とする。
⑥Scratch/Stain on/in glass ガラス傷・汚れ	A scratch,dent,or foreign particles such as stain,attached on the surface or the inside of the front glass. フロントガラス内面・表面のガラス面の傷、シミ等の異物付着	1.Scratch which can be clearly observed through the specified filter should be judged as defect. 指定ﾌｨﾙﾀｰを通して傷のはっきり判る物を不良とする。 2.The criterion for the dent and foreign particle are the same as the specified in ①. 打痕状の傷、異物等は、①頁と同等判定とする。
⑦Chip on the front glass and base plate ガラス欠け	For chip on the front glass and base plate,refer to the next page. ガラス欠けについては、次頁参照	Refer to the next page. 次頁参照

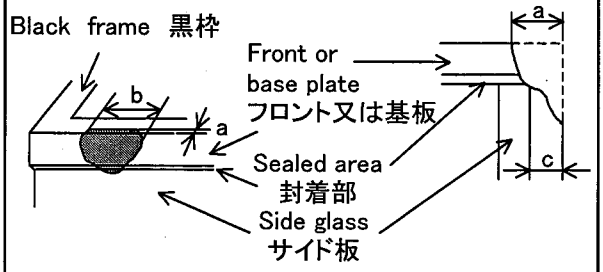
形名 Type No.
16-SD-13GINK

Criterion for the glass chip on the front glass or the base plate.

Definition 定義	Judgment Criterion 判定基準

Black frame 黒枠





a : depth of chipping
欠けの奥行き寸法

b : length of chipping
欠けの長さ寸法

c : chipping size in relation to thickness of the side glass.
サイド板厚に対する欠け寸法

L : package width (length wide)
パッケージ幅（長辺方向）

1) Chipping size Spec. 欠けの寸法規格(mm)

	VFD:a	FLVFD:a	b	c
L≦100	within the black frame 黒枠以内	3.0max.	10max.	1/3max.
L>100	within the black frame 黒枠以内	3.5max.	15max.	1/3max.

VFD : vacuum fluorescent display
蛍光表示管

FLVFD :Front Luminous Vacuum Fluorescent Display
前面発光型蛍光表示管

2) A chip with "a" less than 1mm should not be counted as defect point.
a寸法が1mm未満の場合は欠点としない。

3) A chip area covered with sealing cement should not be counted as defect point.
封着前の欠けは、欠けの中に封着セメントが流入していれば欠点としない。

4) Up to 3 chips within this specification in a same display to be allowed.
表示管全体で規格内の欠け数は3ケまで良品とする。

形名 Type No.
16-SD-13GINK