

Features

- Operating voltage: 2.4V~5.2V
- Built-in 256kHz RC oscillator
- External 32.768kHz crystal or 256kHz frequency source input
- Selection of 1/2 or 1/3 bias, and selection of 1/2 or 1/3 or 1/4 duty LCD applications
- Internal time base frequency sources
- Two selectable buzzer frequencies (2kHz/4kHz)
- Power down command reduces power consumption
- Built-in time base generator and WDT
- Time base or WDT overflow output
- 8 kinds of time base/WDT clock sources
- 32×4 LCD driver
- Built-in 32×4 bit display RAM
- 3-wire serial interface
- Internal LCD driving frequency source
- Software configuration feature
- Data mode and command mode instructions
- R/W address auto increment
- Three data accessing modes
- VLCD pin for adjusting LCD operating voltage
- HT1621: 48-pin SSOP package
- HT1621B: 48-pin DIP/SSOP/LQFP package
- HT1621D: 28-pin SKDIP package
- HT1621G: Gold bumped chip

General Description

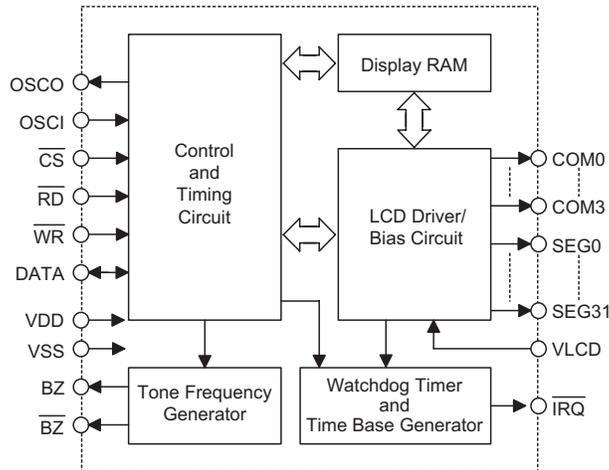
The HT1621 is a 128 pattern (32×4), memory mapping, and multi-function LCD driver. The S/W configuration feature of the HT1621 makes it suitable for multiple LCD applications including LCD modules and display sub-

systems. Only three or four lines are required for the interface between the host controller and the HT1621. The HT1621 contains a power down command to reduce power consumption.

Selection Table

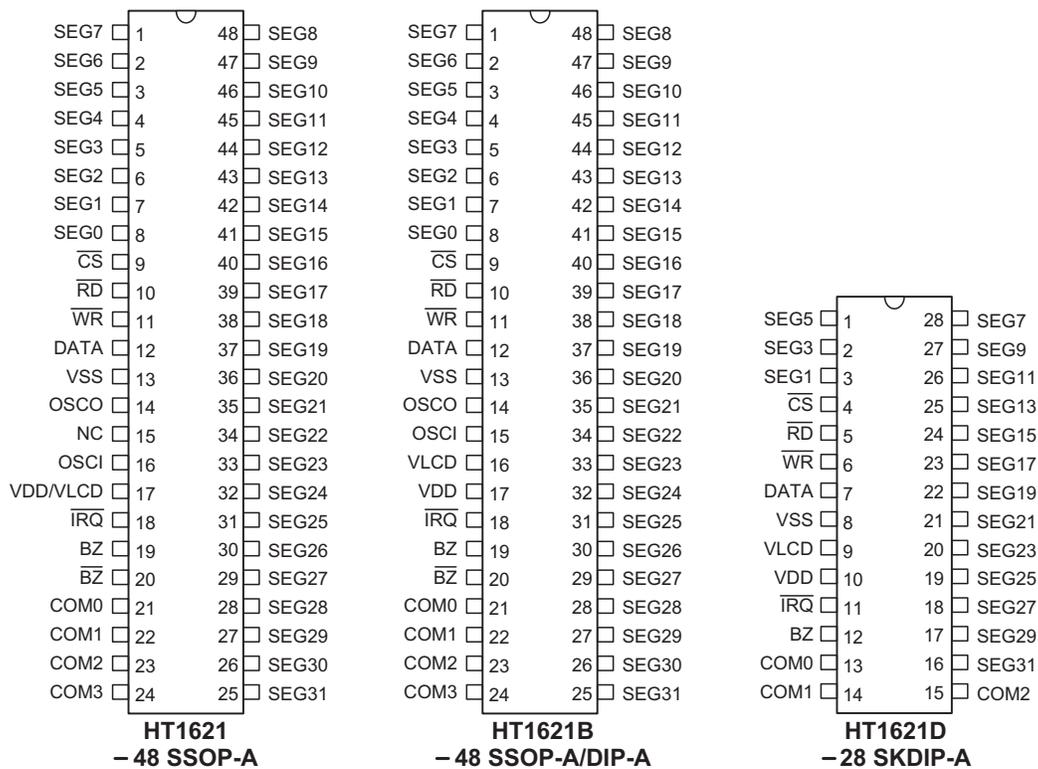
| HT162X | HT1620 | HT1621 | HT1622 | HT16220 | HT1623 | HT1625 | HT1626 |
|---------------|--------|--------|--------|---------|--------|--------|--------|
| COM | 4 | 4 | 8 | 8 | 8 | 8 | 16 |
| SEG | 32 | 32 | 32 | 32 | 48 | 64 | 48 |
| Built-in Osc. | — | √ | √ | — | √ | √ | √ |
| Crystal Osc. | √ | √ | — | √ | √ | √ | √ |

Block Diagram



Note: \overline{CS} : Chip selection
 BZ, \overline{BZ} : Tone outputs
 \overline{WR} , \overline{RD} , DATA: Serial interface
 COM0~COM3, SEG0~SEG31: LCD outputs
 \overline{IRQ} : Time base or WDT overflow output

Pin Assignment



Pad Coordinates

Unit: mil

| Pad No. | X | Y | Pad No. | X | Y |
|---------|--------|--------|---------|--------|--------|
| 1 | -55.04 | 59.46 | 25 | 58.14 | -25.29 |
| 2 | -58.52 | 22.18 | 26 | 58.14 | -18.66 |
| 3 | -58.52 | 15.56 | 27 | 58.14 | -11.94 |
| 4 | -58.52 | 5.36 | 28 | 58.14 | -5.31 |
| 5 | -58.52 | -4.51 | 29 | 58.14 | 1.32 |
| 6 | -58.52 | -11.14 | 30 | 58.14 | 7.95 |
| 7 | -58.52 | -34.76 | 31 | 58.14 | 14.58 |
| 8 | -58.52 | -41.90 | 32 | 58.14 | 21.21 |
| 9 | -58.52 | -49.13 | 33 | 55.55 | 59.46 |
| 10 | -58.52 | -59.08 | 34 | 48.92 | 59.46 |
| 11 | -44.07 | -59.08 | 35 | 42.29 | 59.46 |
| 12 | -31.58 | -59.08 | 36 | 35.66 | 59.46 |
| 13 | -20.70 | -59.08 | 37 | 29.03 | 59.46 |
| 14 | -13.98 | -59.08 | 38 | 22.40 | 59.46 |
| 15 | -7.05 | -59.08 | 39 | 15.77 | 59.46 |
| 16 | -0.34 | -59.08 | 40 | 9.14 | 59.46 |
| 17 | 6.33 | -59.08 | 41 | 2.42 | 59.46 |
| 18 | 12.96 | -59.08 | 42 | -4.21 | 59.46 |
| 19 | 19.59 | -59.08 | 43 | -10.84 | 59.46 |
| 20 | 58.14 | -58.44 | 44 | -17.47 | 59.46 |
| 21 | 58.14 | -51.81 | 45 | -24.10 | 59.46 |
| 22 | 58.14 | -45.18 | 46 | -30.73 | 59.46 |
| 23 | 58.14 | -38.55 | 47 | -38.17 | 59.46 |
| 24 | 58.14 | -31.92 | 48 | -45.39 | 59.46 |

Pad Description

| Pad No. | Pad Name | I/O | Function |
|---------|---------------------|-----|---|
| 1 | \overline{CS} | I | Chip selection input with pull-high resistor When the \overline{CS} is logic high, the data and command read from or written to the HT1621 are disabled. The serial interface circuit is also reset. But if \overline{CS} is at logic low level and is input to the \overline{CS} pad, the data and command transmission between the host controller and the HT1621 are all enabled. |
| 2 | \overline{RD} | I | READ clock input with pull-high resistor Data in the RAM of the HT1621 are clocked out on the falling edge of the \overline{RD} signal. The clocked out data will appear on the DATA line. The host controller can use the next rising edge to latch the clocked out data. |
| 3 | \overline{WR} | I | WRITE clock input with pull-high resistor Data on the DATA line are latched into the HT1621 on the rising edge of the \overline{WR} signal. |
| 4 | DATA | I/O | Serial data input/output with pull-high resistor |
| 5 | VSS | — | Negative power supply, ground |
| 7 | OSCI | I | The OSCI and OSCO pads are connected to a 32.768kHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on-chip RC oscillator is selected instead, the OSCI and OSCO pads can be left open. |
| 6 | OSCO | O | |
| 8 | VLCD | I | LCD power input |
| 9 | VDD | — | Positive power supply |
| 10 | \overline{IRQ} | O | Time base or WDT overflow flag, NMOS open drain output |
| 11, 12 | BZ, \overline{BZ} | O | 2kHz or 4kHz tone frequency output pair |
| 13~16 | COM0~COM3 | O | LCD common outputs |
| 48~17 | SEG0~SEG31 | O | LCD segment outputs |

Absolute Maximum Ratings

Supply Voltage $V_{SS}-0.3V$ to $V_{SS}+5.5V$ Storage Temperature $-50^{\circ}C$ to $125^{\circ}C$
 Input Voltage..... $V_{SS}-0.3V$ to $V_{DD}+0.3V$ Operating Temperature..... $-25^{\circ}C$ to $75^{\circ}C$

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

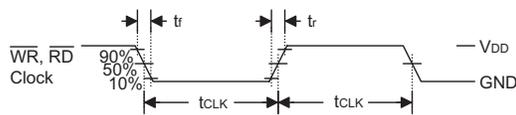
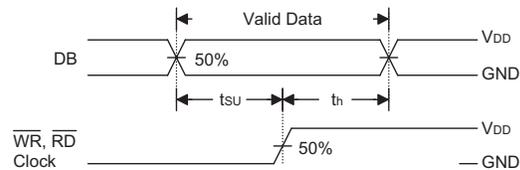
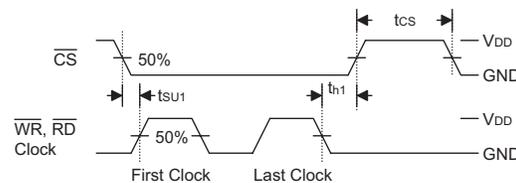
Ta=25°C

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|------------------|--|-----------------|---|------|------|------|------|
| | | V _{DD} | Conditions | | | | |
| V _{DD} | Operating Voltage | — | — | 2.4 | — | 5.2 | V |
| I _{DD1} | Operating Current | 3V | No load/LCD ON | — | 150 | 300 | μA |
| | | 5V | On-chip RC oscillator | — | 300 | 600 | μA |
| I _{DD2} | Operating Current | 3V | No load/LCD ON | — | 60 | 120 | μA |
| | | 5V | Crystal oscillator | — | 120 | 240 | μA |
| I _{DD3} | Operating Current | 3V | No load/LCD ON | — | 100 | 200 | μA |
| | | 5V | External clock source | — | 200 | 400 | μA |
| I _{STB} | Standby Current | 3V | No load, Power down mode | — | 0.1 | 5 | μA |
| | | 5V | | — | 0.3 | 10 | μA |
| V _{IL} | Input Low Voltage | 3V | DATA, \overline{WR} , \overline{CS} , \overline{RD} | 0 | — | 0.6 | V |
| | | 5V | | 0 | — | 1.0 | V |
| V _{IH} | Input High Voltage | 3V | DATA, \overline{WR} , \overline{CS} , \overline{RD} | 2.4 | — | 3.0 | V |
| | | 5V | | 4.0 | — | 5.0 | V |
| I _{OL1} | DATA, BZ, \overline{BZ} , \overline{IRQ} | 3V | V _{OL} =0.3V | 0.5 | 1.2 | — | mA |
| | | 5V | V _{OL} =0.5V | 1.3 | 2.6 | — | mA |
| I _{OH1} | DATA, BZ, \overline{BZ} | 3V | V _{OH} =2.7V | -0.4 | -0.8 | — | mA |
| | | 5V | V _{OH} =4.5V | -0.9 | -1.8 | — | mA |
| I _{OL2} | LCD Common Sink Current | 3V | V _{OL} =0.3V | 80 | 150 | — | μA |
| | | 5V | V _{OL} =0.5V | 150 | 250 | — | μA |
| I _{OH2} | LCD Common Source Current | 3V | V _{OH} =2.7V | -80 | -120 | — | μA |
| | | 5V | V _{OH} =4.5V | -120 | -200 | — | μA |
| I _{OL3} | LCD Segment Sink Current | 3V | V _{OL} =0.3V | 60 | 120 | — | μA |
| | | 5V | V _{OL} =0.5V | 120 | 200 | — | μA |
| I _{OH3} | LCD Segment Source Current | 3V | V _{OH} =2.7V | -40 | -70 | — | μA |
| | | 5V | V _{OH} =4.5V | -70 | -100 | — | μA |
| R _{PH} | Pull-high Resistor | 3V | DATA, \overline{WR} , \overline{CS} , \overline{RD} | 40 | 80 | 150 | kΩ |
| | | 5V | | 30 | 60 | 100 | kΩ |

A.C. Characteristics

Ta=25°C

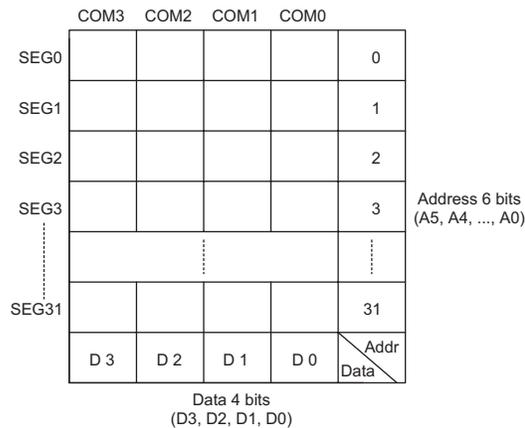
| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---------------------------------|--|-----------------|-----------------------|------|-------------------------|------|------|
| | | V _{DD} | Conditions | | | | |
| f _{SYS1} | System Clock | — | On-chip RC oscillator | — | 256 | — | kHz |
| f _{SYS2} | System Clock | — | Crystal oscillator | — | 32.768 | — | kHz |
| f _{SYS3} | System Clock | — | External clock source | — | 256 | — | kHz |
| f _{LCD} | LCD Clock | — | On-chip RC oscillator | — | f _{SYS1} /1024 | — | Hz |
| | | — | Crystal oscillator | — | f _{SYS2} /128 | — | Hz |
| | | — | External clock source | — | f _{SYS3} /1024 | — | Hz |
| t _{COM} | LCD Common Period | — | n: Number of COM | — | n/f _{LCD} | — | s |
| f _{CLK1} | Serial Data Clock (\overline{WR} pin) | 3V | Duty cycle 50% | — | — | 150 | kHz |
| | | 5V | | — | — | 300 | kHz |
| f _{CLK2} | Serial Data Clock (\overline{RD} pin) | 3V | Duty cycle 50% | — | — | 75 | kHz |
| | | 5V | | — | — | 150 | kHz |
| f _{TONE} | Tone Frequency | — | On-chip RC oscillator | — | 2.0 or 4.0 | — | kHz |
| t _{CS} | Serial Interface Reset Pulse Width (Figure 3) | — | \overline{CS} | — | 250 | — | ns |
| t _{CLK} | \overline{WR} , \overline{RD} Input Pulse Width (Figure 1) | 3V | Write mode | 3.34 | — | — | μs |
| | | | Read mode | 6.67 | — | — | |
| | | 5V | Write mode | 1.67 | — | — | μs |
| | | | Read mode | 3.34 | — | — | |
| t _r , t _f | Rise/Fall Time Serial Data Clock Width (Figure 1) | — | — | — | 120 | — | ns |
| t _{su} | Setup Time for DATA to \overline{WR} , \overline{RD} Clock Width (Figure 2) | — | — | — | 120 | — | ns |
| t _h | Hold Time for DATA to \overline{WR} , \overline{RD} Clock Width (Figure 2) | — | — | — | 120 | — | ns |
| t _{su1} | Setup Time for \overline{CS} to \overline{WR} , \overline{RD} Clock Width (Figure 3) | — | — | — | 100 | — | ns |
| t _{h1} | Hold Time for \overline{CS} to \overline{WR} , \overline{RD} Clock Width (Figure 3) | — | — | — | 100 | — | ns |


Figure 1

Figure 2

Figure 3

Functional Description

Display Memory – RAM

The static display memory (RAM) is organized into 32x4 bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE, and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD pattern:



RAM Mapping

System Oscillator

The HT1621 system clock is used to generate the time base/Watchdog Timer (WDT) clock frequency, LCD driving clock, and tone frequency. The source of the clock may be from an on-chip RC oscillator (256kHz), a crystal oscillator (32.768kHz), or an external 256kHz clock by the S/W setting. The configuration of the system oscillator is as shown. After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. That command is, however, available only for the on-chip RC oscillator or for the crystal oscillator. Once the system clock stops, the LCD display will become blank, and the time base/WDT lose its function as well.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS

command reduces power consumption, serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor carry out the power down mode. The crystal oscillator option can be applied to connect an external frequency source of 32kHz to the OSCI pin. In this case, the system fails to enter the power down mode, similar to the case in the external 256kHz clock source operation. At the initial system power on, the HT1621 is at the SYS DIS state.

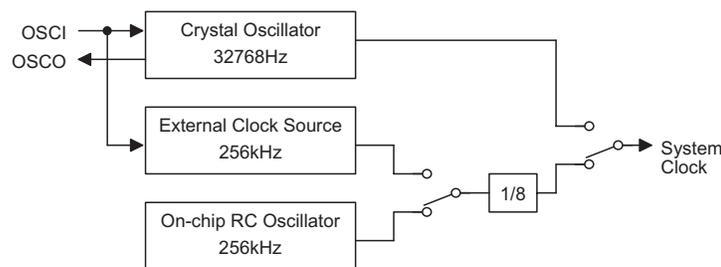
Time Base and Watchdog Timer (WDT)

The time base generator is comprised by an 8-stage count-up ripple counter and is designed to generate an accurate time base. The watch dog timer (WDT), on the other hand, is composed of an 8-stage time base generator along with a 2-stage count-up counter, and is designed to break the host controller or other subsystems from abnormal states such as unknown or unwanted jump, execution errors, etc. The WDT time-out will result in the setting of an internal WDT time-out flag. The outputs of the time base generator and of the WDT time-out flag can be connected to the IRQ output by a command option. There are totally eight frequency sources available for the time base generator and the WDT clock. The frequency is calculated by the following equation.

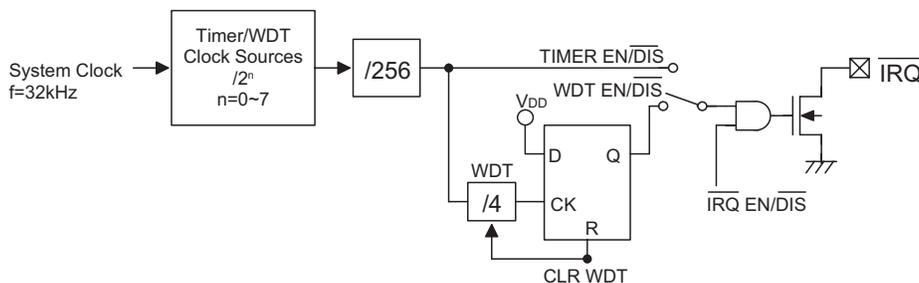
$$f_{WDT} = \frac{32kHz}{2^n}$$

where the value of n ranges from 0 to 7 by command options. The 32kHz in the above equation indicates that the source of the system frequency is derived from a crystal oscillator of 32.768kHz, an on-chip oscillator (256kHz), or an external frequency of 256kHz.

If an on-chip oscillator (256kHz) or an external 256kHz frequency is chosen as the source of the system frequency, the frequency source is by default prescaled to 32kHz by a 3-stage prescaler. Employing both the time base generator and the WDT related commands, one should be careful since the time base generator and WDT share the same 8-stage counter. For example, invoking the WDT DIS command disables the time base generator whereas executing the WDT EN command



System Oscillator Configuration



Timer and WDT Configurations

not only enables the time base generator but activates the WDT time-out flag output (connect the WDT time-out flag to the $\overline{\text{IRQ}}$ pin). After the $\overline{\text{TIMER EN}}$ command is transferred, the WDT is disconnected from the $\overline{\text{IRQ}}$ pin, and the output of the time base generator is connected to the $\overline{\text{IRQ}}$ pin. The WDT can be cleared by executing the CLR WDT command, and the contents of the time base generator is cleared by executing the CLR WDT or the CLR TIMER command. The CLR WDT or the CLR TIMER command should be executed prior to the WDT EN or the $\overline{\text{TIMER EN}}$ command respectively. Before executing the $\overline{\text{IRQ EN}}$ command the CLR WDT or CLR TIMER command should be executed first. The CLR TIMER command has to be executed before switching from the WDT mode to the time base mode. Once the WDT time-out occurs, the $\overline{\text{IRQ}}$ pin will stay at a logic low level until the CLR WDT or the $\overline{\text{IRQ DIS}}$ command is issued. After the $\overline{\text{IRQ}}$ output is disabled the $\overline{\text{IRQ}}$ pin will remain at the floating state. The $\overline{\text{IRQ}}$ output can be enabled or disabled by executing the $\overline{\text{IRQ EN}}$ or the $\overline{\text{IRQ DIS}}$ command, respectively. The $\overline{\text{IRQ EN}}$ makes the output of the time base generator or of the WDT time-out flag appear on the $\overline{\text{IRQ}}$ pin. The configuration of the time base generator along with the WDT are as shown. In the case of on-chip RC oscillator or crystal oscillator, the power down mode can reduce power consumption since the oscillator can be turned on or off by the corresponding system commands. At the power down mode the time base/WDT loses all its functions.

On the other hand, if an external clock is selected as the source of system frequency the $\overline{\text{SYS DIS}}$ command turns out invalid and the power down mode fails to be carried out. That is, after the external clock source is selected, the HT1621 will continue working until system

power fails or the external clock source is removed. After the system power on, the $\overline{\text{IRQ}}$ will be disabled.

Tone Output

A simple tone generator is implemented in the HT1621. The tone generator can output a pair of differential driving signals on the BZ and $\overline{\text{BZ}}$, which are used to generate a single tone. By executing the TONE4K and TONE2K commands there are two tone frequency outputs selectable. The TONE4K and TONE2K commands set the tone frequency to 4kHz and 2kHz, respectively. The tone output can be turned on or off by invoking the TONE ON or the TONE OFF command. The tone outputs, namely BZ and $\overline{\text{BZ}}$, are a pair of differential driving outputs used to drive a piezo buzzer. Once the system is disabled or the tone output is inhibited, the BZ and the $\overline{\text{BZ}}$ outputs will remain at low level.

LCD Driver

The HT1621 is a 128 (32x4) pattern LCD driver. It can be configured as 1/2 or 1/3 bias and 2 or 3 or 4 commons of LCD driver by the S/W configuration. This feature makes the HT1621 suitable for multiply LCD applications. The LCD driving clock is derived from the system clock. The value of the driving clock is always 256Hz even when it is at a 32.768kHz crystal oscillator frequency, an on-chip RC oscillator frequency, or an external frequency. The LCD corresponding commands are summarized in the table.

The bold form of 1 0 0, namely **1 0 0**, indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command, will be omitted. The LCD OFF command turns the LCD display off by disabling the LCD bias gen-

| Name | Command Code | Function |
|------------|--------------------------------|---|
| LCD OFF | 1 0 0 0 0 0 0 0 1 0 X | Turn off LCD outputs |
| LCD ON | 1 0 0 0 0 0 0 0 1 1 X | Turn on LCD outputs |
| BIAS & COM | 1 0 0 0 0 1 0 a b X c X | c=0: 1/2 bias option c=1: 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option |

erator. The LCD ON command, on the other hand, turns the LCD display on by enabling the LCD bias generator. The BIAS and COM are the LCD panel related commands. Using the LCD related commands, the HT1621 can be compatible with most types of LCD panels.

Command Format

The HT1621 can be configured by the S/W setting. There are two mode commands to configure the HT1621 resources and to transfer the LCD display data. The configuration mode of the HT1621 is called command mode, and its command mode ID is **1 0 0**. The command mode consists of a system configuration command, a system frequency selection command, a LCD configuration command, a tone frequency selection command, a timer/WDT setting command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations. The following are the data mode IDs and the command mode ID:

| Operation | Mode | ID |
|-------------------|---------|-------|
| Read | Data | 1 1 0 |
| Write | Data | 1 0 1 |
| Read-Modify-Write | Data | 1 0 1 |
| Command | Command | 1 0 0 |

The mode command should be issued before the data or command is transferred. If successive commands have been issued, the command mode ID, namely **1 0 0**, can be omitted. While the system is operating in the non-successive command or the non-successive ad-

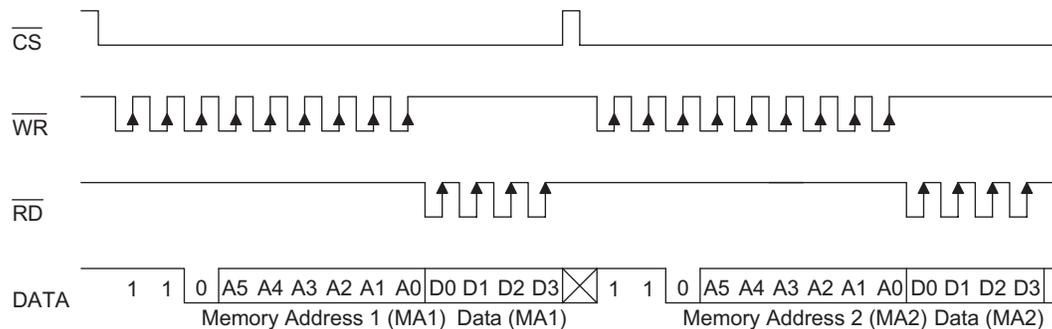
dress data mode, the \overline{CS} pin should be set to "1" and the previous operation mode will be reset also. Once the \overline{CS} pin returns to "0" a new operation mode ID should be issued first.

Interfacing

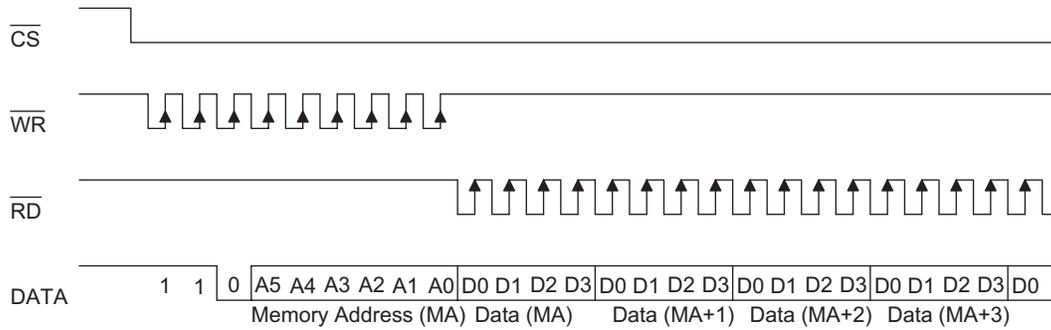
Only four lines are required to interface with the HT1621. The \overline{CS} line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the HT1621. If the \overline{CS} pin is set to 1, the data and command issued between the host controller and the HT1621 are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the HT1621. The DATA line is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line. The \overline{RD} line is the READ clock input. Data in the RAM are clocked out on the falling edge of the \overline{RD} signal, and the clocked out data will then appear on the DATA line. It is recommended that the host controller read in correct data during the interval between the rising edge and the next falling edge of the \overline{RD} signal. The \overline{WR} line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the HT1621 on the rising edge of the \overline{WR} signal. There is an optional IRQ line to be used as an interface between the host controller and the HT1621. The \overline{IRQ} pin can be selected as a timer output or a WDT overflow flag output by the S/W setting. The host controller can perform the time base or the WDT function by being connected with the \overline{IRQ} pin of the HT1621.

Timing Diagrams

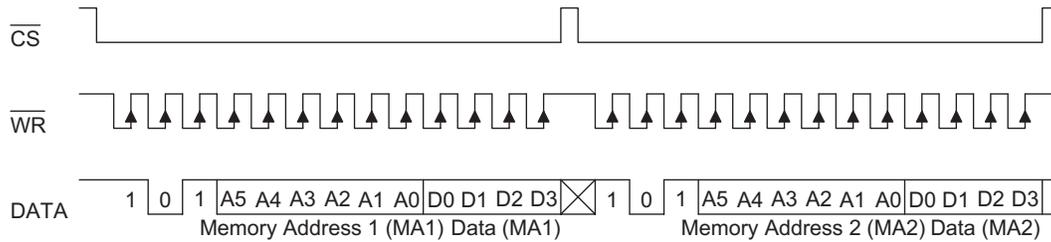
READ Mode (Command Code : 1 1 0)



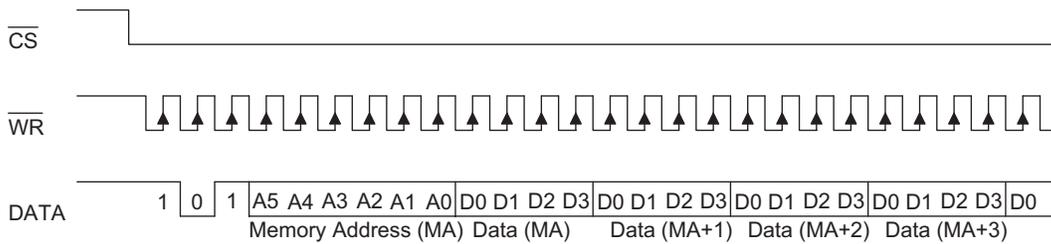
READ Mode (Successive Address Reading)



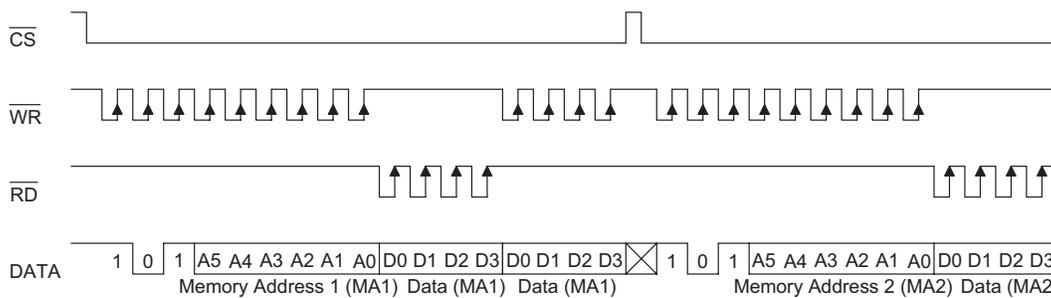
WRITE Mode (Command Code : 1 0 1)



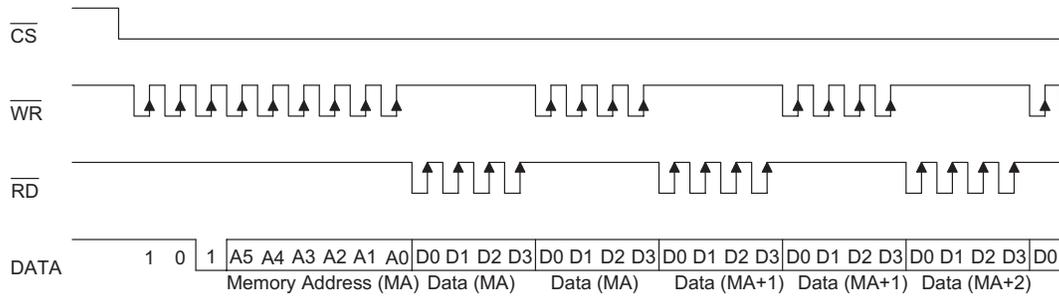
WRITE Mode (Successive Address Writing)



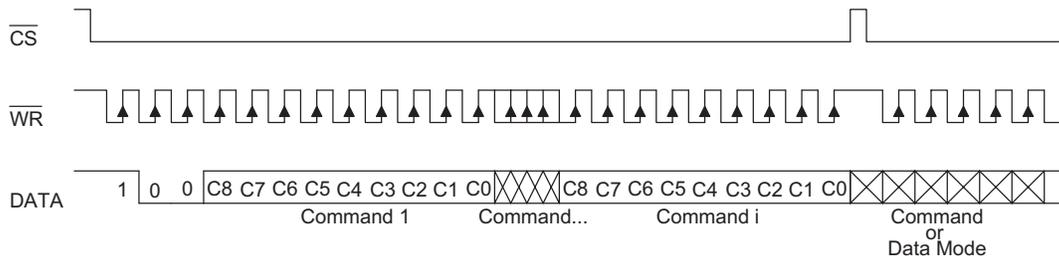
Read-Modify-Write Mode (Command Code : 1 0 1)



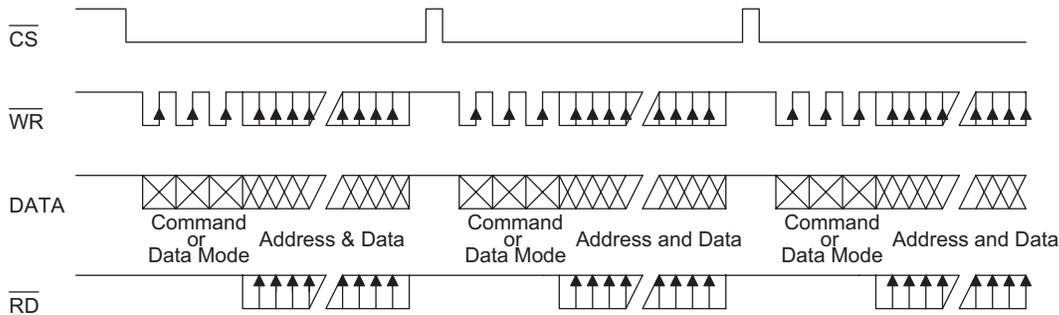
Read-Modify-Write Mode (Successive Address Accessing)



Command Mode (Command Code : 1 0 0)



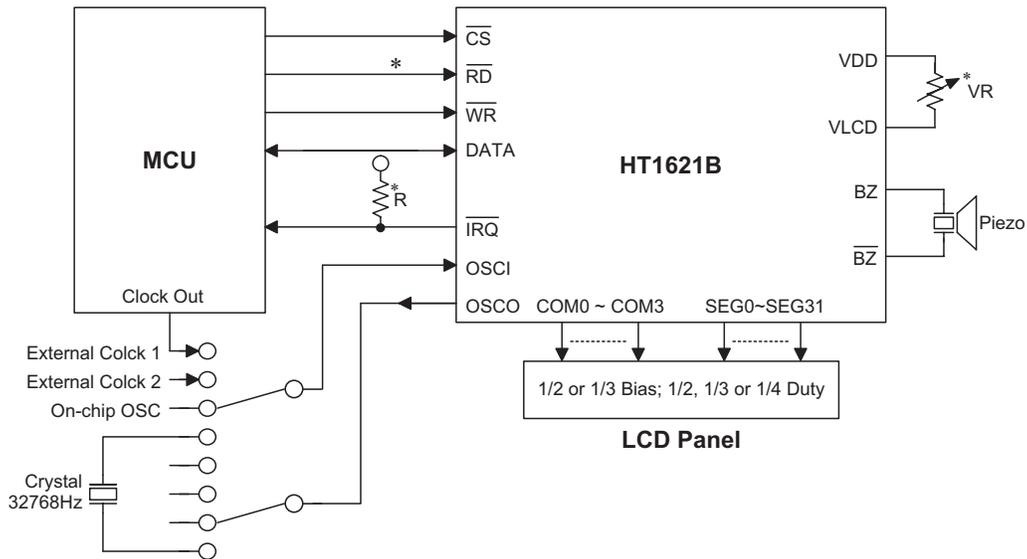
Mode (Data And Command Mode)



Note: It is recommended that the host controller should read in the data from the DATA line between the rising edge of the \overline{RD} line and the falling edge of the next \overline{RD} line.

Application Circuits

Host Controller with an HT1621 Display System



Note: The connection of \overline{IRQ} and \overline{RD} pin can be selected depending on the requirement of the MCU.

The voltage applied to V_{LCD} pin must be lower than V_{DD} .

Adjust VR to fit LCD display, at $V_{DD}=5V$, $V_{LCD}=4V$, $VR=15k\Omega\pm 20\%$.

Adjust R (external pull-high resistance) to fit user's time base clock.

Command Summary

| Name | ID | Command Code | D/C | Function | Def. |
|-------------------|-------|----------------------|-----|--|------|
| READ | 1 1 0 | A5A4A3A2A1A0D0D1D2D3 | D | Read data from the RAM | |
| WRITE | 1 0 1 | A5A4A3A2A1A0D0D1D2D3 | D | Write data to the RAM | |
| READ-MODIFY-WRITE | 1 0 1 | A5A4A3A2A1A0D0D1D2D3 | D | READ and WRITE to the RAM | |
| SYS DIS | 1 0 0 | 0000-0000-X | C | Turn off both system oscillator and LCD bias generator | Yes |
| SYS EN | 1 0 0 | 0000-0001-X | C | Turn on system oscillator | |
| LCD OFF | 1 0 0 | 0000-0010-X | C | Turn off LCD bias generator | Yes |
| LCD ON | 1 0 0 | 0000-0011-X | C | Turn on LCD bias generator | |
| TIMER DIS | 1 0 0 | 0000-0100-X | C | Disable time base output | |
| WDT DIS | 1 0 0 | 0000-0101-X | C | Disable WDT time-out flag output | |
| TIMER EN | 1 0 0 | 0000-0110-X | C | Enable time base output | |
| WDT EN | 1 0 0 | 0000-0111-X | C | Enable WDT time-out flag output | |
| TONE OFF | 1 0 0 | 0000-1000-X | C | Turn off tone outputs | Yes |
| TONE ON | 1 0 0 | 0000-1001-X | C | Turn on tone outputs | |
| CLR TIMER | 1 0 0 | 0000-11XX-X | C | Clear the contents of time base generator | |
| CLR WDT | 1 0 0 | 0000-111X-X | C | Clear the contents of WDT stage | |
| XTAL 32K | 1 0 0 | 0001-01XX-X | C | System clock source, crystal oscillator | |

| Name | ID | Command Code | D/C | Function | Def. |
|-----------------------------|--------------|--------------|-----|--|------|
| RC 256K | 1 0 0 | 0001-10XX-X | C | System clock source, on-chip RC oscillator | Yes |
| EXT 256K | 1 0 0 | 0001-11XX-X | C | System clock source, external clock source | |
| BIAS 1/2 | 1 0 0 | 0010-abX0-X | C | LCD 1/2 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option | |
| BIAS 1/3 | 1 0 0 | 0010-abX1-X | C | LCD 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option | |
| TONE 4K | 1 0 0 | 010X-XXXX-X | C | Tone frequency, 4kHz | |
| TONE 2K | 1 0 0 | 011X-XXXX-X | C | Tone frequency, 2kHz | |
| $\overline{\text{IRQ}}$ DIS | 1 0 0 | 100X-0XXX-X | C | Disable $\overline{\text{IRQ}}$ output | Yes |
| $\overline{\text{IRQ}}$ EN | 1 0 0 | 100X-1XXX-X | C | Enable $\overline{\text{IRQ}}$ output | |
| F1 | 1 0 0 | 101X-X000-X | C | Time base/WDT clock output:1Hz The WDT time-out flag after: 4s | |
| F2 | 1 0 0 | 101X-X001-X | C | Time base/WDT clock output:2Hz The WDT time-out flag after: 2s | |
| F4 | 1 0 0 | 101X-X010-X | C | Time base/WDT clock output:4Hz The WDT time-out flag after: 1s | |
| F8 | 1 0 0 | 101X-X011-X | C | Time base/WDT clock output:8Hz The WDT time-out flag after: 1/2s | |
| F16 | 1 0 0 | 101X-X100-X | C | Time base/WDT clock output:16Hz The WDT time-out flag after: 1/4s | |
| F32 | 1 0 0 | 101X-X101-X | C | Time base/WDT clock output:32Hz The WDT time-out flag after: 1/8s | |
| F64 | 1 0 0 | 101X-X110-X | C | Time base/WDT clock output:64Hz The WDT time-out flag after: 1/16s | |
| F128 | 1 0 0 | 101X-X111-X | C | Time base/WDT clock output:128Hz The WDT time-out flag after: 1/32s | Yes |
| TEST | 1 0 0 | 1110-0000-X | C | Test mode, user don't use. | |
| NORMAL | 1 0 0 | 1110-0011-X | C | Normal mode | Yes |

Note: X : Don't care

A5~A0 : RAM addresses

D3~D0 : RAM data

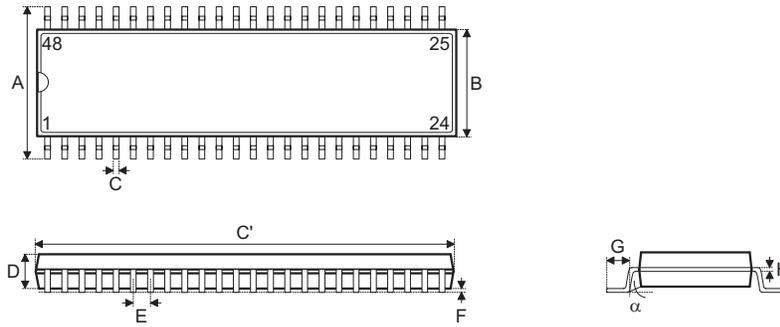
D/C : Data/command mode

Def. : Power on reset default

All the bold forms, namely **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Of these, **1 0 0** indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base/WDT clock frequency can be derived from an on-chip 256kHz RC oscillator, a 32.768kHz crystal oscillator, or an external 256kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the HT1621 after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the HT1621.

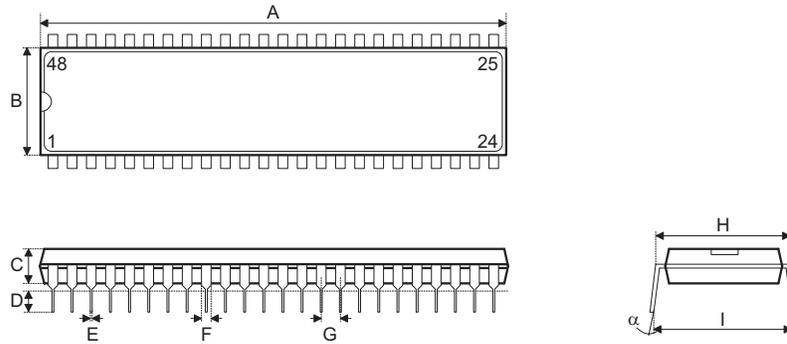
Package Information

48-pin SSOP (300mil) Outline Dimensions



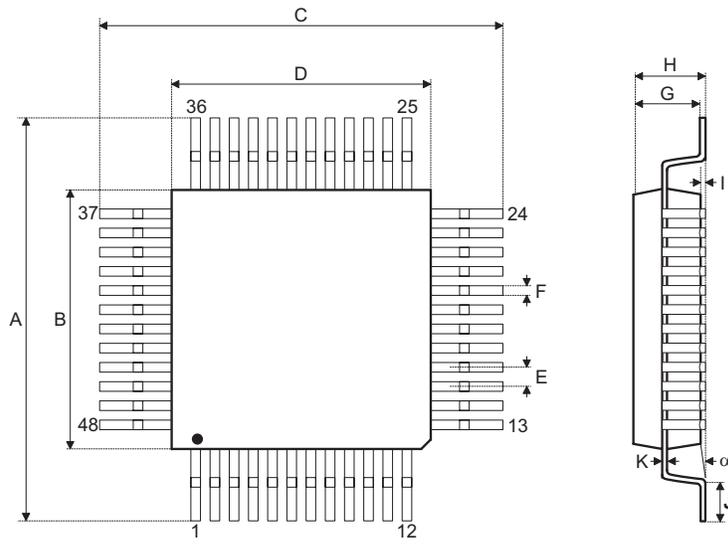
| Symbol | Dimensions in mil | | |
|----------|-------------------|------|------|
| | Min. | Nom. | Max. |
| A | 395 | — | 420 |
| B | 291 | — | 299 |
| C | 8 | — | 12 |
| C' | 613 | — | 637 |
| D | 85 | — | 99 |
| E | — | 25 | — |
| F | 4 | — | 10 |
| G | 25 | — | 35 |
| H | 4 | — | 12 |
| α | 0° | — | 8° |

48-pin DIP (600mil) Outline Dimensions



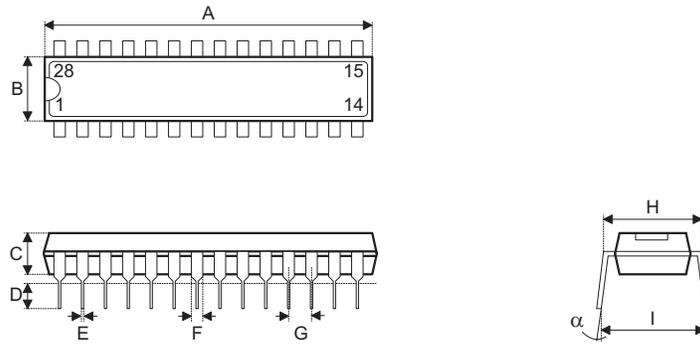
| Symbol | Dimensions in mil | | |
|----------|-------------------|------|------|
| | Min. | Nom. | Max. |
| A | 2435 | — | 2445 |
| B | 535 | — | 555 |
| C | 145 | — | 155 |
| D | 125 | — | 145 |
| E | 16 | — | 20 |
| F | 50 | — | 70 |
| G | — | 100 | — |
| H | 595 | — | 615 |
| I | 635 | — | 670 |
| α | 0° | — | 15° |

48-pin LQFP (7x7) Outline Dimensions



| Symbol | Dimensions in mm | | |
|--------|------------------|------|------|
| | Min. | Nom. | Max. |
| A | 8.90 | — | 9.10 |
| B | 6.90 | — | 7.10 |
| C | 8.90 | — | 9.10 |
| D | 6.90 | — | 7.10 |
| E | — | 0.50 | — |
| F | — | 0.20 | — |
| G | 1.35 | — | 1.45 |
| H | — | — | 1.60 |
| I | — | 0.10 | — |
| J | 0.45 | — | 0.75 |
| K | 0.10 | — | 0.20 |
| α | 0° | — | 7° |

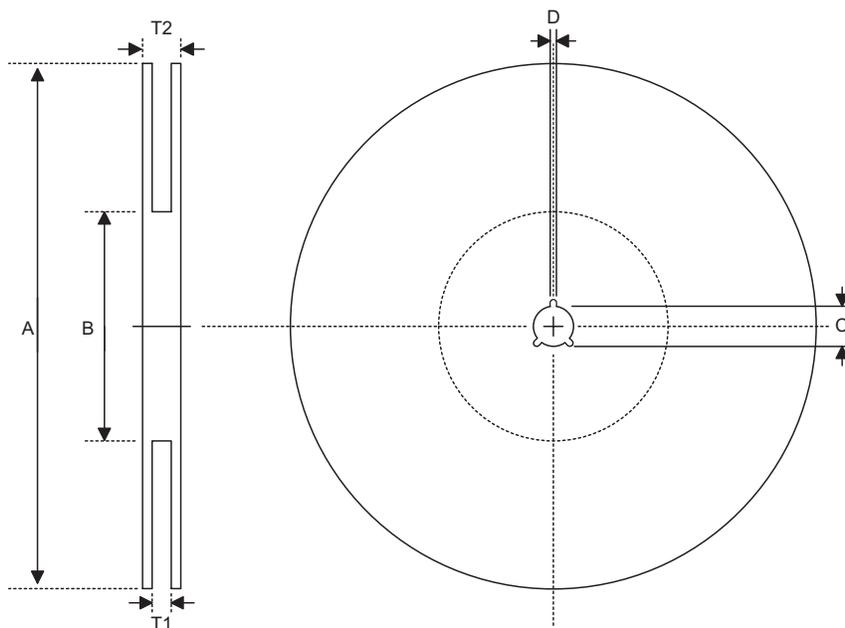
28-pin SKDIP (300mil) Outline Dimensions



| Symbol | Dimensions in mil | | |
|----------|-------------------|------|------|
| | Min. | Nom. | Max. |
| A | 1375 | — | 1395 |
| B | 278 | — | 298 |
| C | 125 | — | 135 |
| D | 125 | — | 145 |
| E | 16 | — | 20 |
| F | 50 | — | 70 |
| G | — | 100 | — |
| H | 295 | — | 315 |
| I | 330 | — | 375 |
| α | 0° | — | 15° |

Product Tape and Reel Specifications

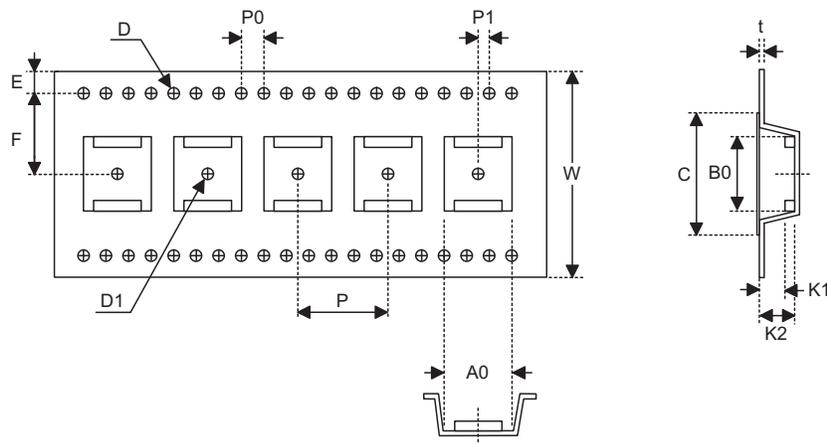
Reel Dimensions



SSOP 48W

| Symbol | Description | Dimensions in mm |
|--------|-----------------------|------------------|
| A | Reel Outer Diameter | 330±1.0 |
| B | Reel Inner Diameter | 100±0.1 |
| C | Spindle Hole Diameter | 13.0+0.5 -0.2 |
| D | Key Slit Width | 2.0±0.5 |
| T1 | Space Between Flange | 32.2+0.3 -0.2 |
| T2 | Reel Thickness | 38.2±0.2 |

Carrier Tape Dimensions



SSOP 48W

| Symbol | Description | Dimensions in mm |
|--------|--|------------------|
| W | Carrier Tape Width | 32.0±0.3 |
| P | Cavity Pitch | 16.0±0.1 |
| E | Perforation Position | 1.75±0.1 |
| F | Cavity to Perforation (Width Direction) | 14.2±0.1 |
| D | Perforation Diameter | 2.0 Min. |
| D1 | Cavity Hole Diameter | 1.5+0.25 |
| P0 | Perforation Pitch | 4.0±0.1 |
| P1 | Cavity to Perforation (Length Direction) | 2.0±0.1 |
| A0 | Cavity Length | 12.0±0.1 |
| B0 | Cavity Width | 16.20±0.1 |
| K1 | Cavity Depth | 2.4±0.1 |
| K2 | Cavity Depth | 3.2±0.1 |
| t | Carrier Tape Thickness | 0.35±0.05 |
| C | Cover Tape Width | 25.5 |

Holtek Semiconductor Inc. (Headquarters)

No.3, Creation Rd. II, Science Park, Hsinchu, Taiwan
Tel: 886-3-563-1999
Fax: 886-3-563-1189
<http://www.holtek.com.tw>

Holtek Semiconductor Inc. (Sales Office)

4F-2, No. 3-2, YuanQu St., Nankang Software Park, Taipei 115, Taiwan
Tel: 886-2-2655-7070
Fax: 886-2-2655-7373
Fax: 886-2-2655-7383 (International sales hotline)

Holtek Semiconductor (Shanghai) Inc.

7th Floor, Building 2, No.889, Yi Shan Rd., Shanghai, China
Tel: 021-6485-5560
Fax: 021-6485-0313
<http://www.holtek.com.cn>

Holtek Semiconductor (Hong Kong) Ltd.

Block A, 3/F, Tin On Industrial Building, 777-779 Cheung Sha Wan Rd., Kowloon, Hong Kong
Tel: 852-2-745-8288
Fax: 852-2-742-8657

Holmate Semiconductor, Inc.

46712 Fremont Blvd., Fremont, CA 94538
Tel: 510-252-9880
Fax: 510-252-9885
<http://www.holmate.com>

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