AS1130

132-LED Cross-Plexing Driver with Scrolling Function

General Description

The AS1130 is a compact LED driver for 132 single LEDs. The devices can be programmed via an I^2C compatible interface. The AS1130 offers a 12x11 LED-matrix with 1/12 cycle rate. The required lines to drive all 132 LEDs are reduced to 12 by using the cross-plexing feature optimizing space on the PCB. The whole LED-matrix driving 132 LEDs can be analog dimmed from 0mA to 30mA in 256 steps (8 bit).

Additionally each of the 132 LEDs can be dimmed individually with 8-bit allowing 256 steps of linear dimming. To reduce CPU usage up to 6 frames can be stored with individual time delays between frames to play small animations automatically.

The AS1130 operates from 2.7V to 5.5V and features a very low shutdown and operational current.

The device offers a programmable IRQ pin. Via a register it can be set on what event (CP_Request, Interface Timeout, Error-detection, POR, End of Frame or End of Movie) the IRQ is triggered.

Also hardware scroll function is implemented in the AS1130.

The device is available in an ultrasmall 20-Pin WL-CSP and an easy to solder 28-pin SSOP/TSSOP package.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS1130, 132-LED Cross-Plexing Driver with Scrolling Function are listed below:

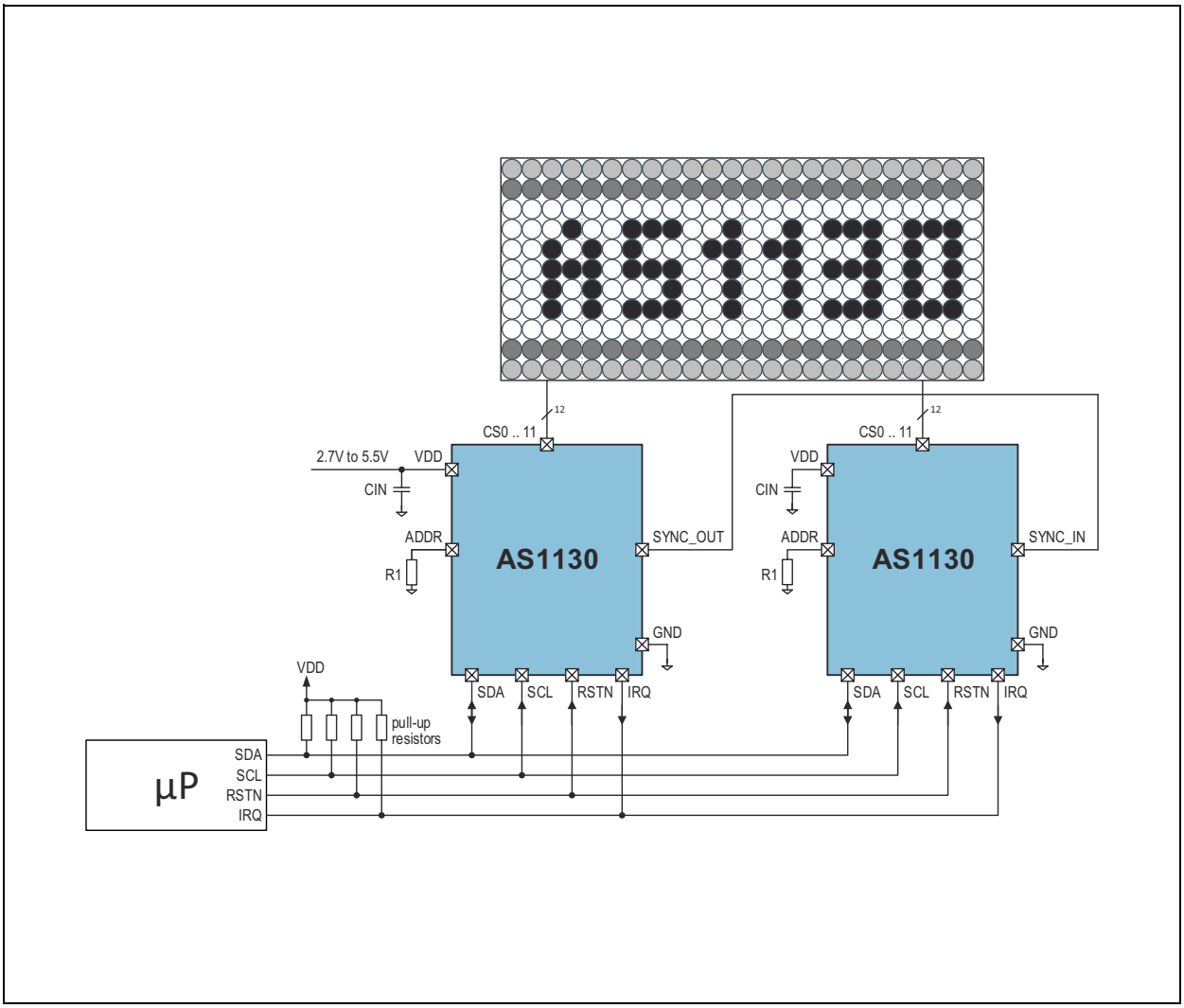
Figure 1:
Added Value of Using AS1130

Benefits	Features
• Worlds lowest PCB real estate vs LED count	• Up to 132 LEDs in a 12x11 matrix
• 16.7M full color matrix with white balance	• 8-bit PWM per LED and current control per line
• Reduces MCU load and increases battery lifetime	• 36 frames of memory with scrolling option
• Identifies defect LEDs and “removes” them from the matrix	• Error detection and correction

Applications

The AS1130 is ideal for dot matrix displays in mobile phones, personal electronics and toys.

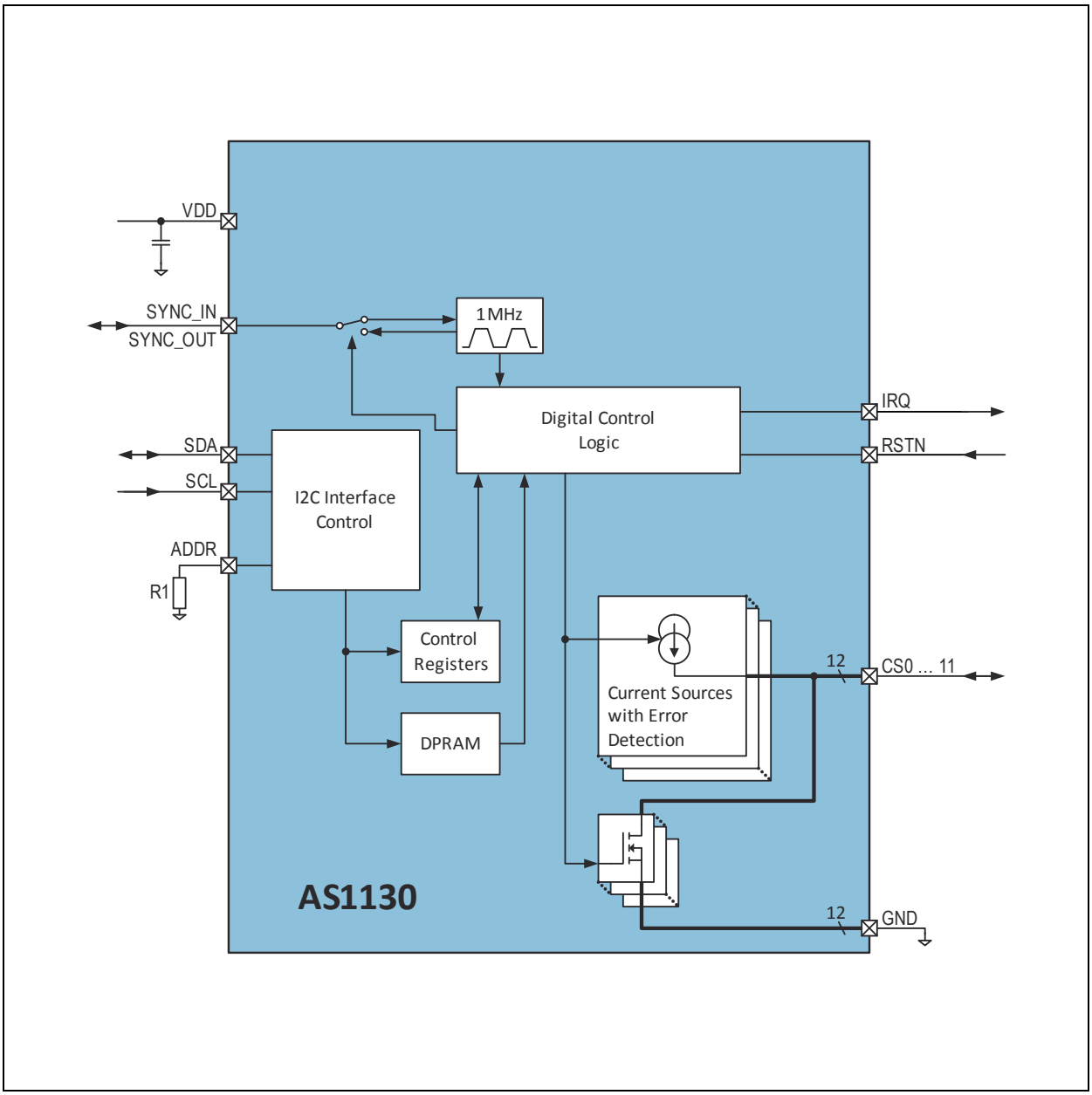
Figure 2:
AS1130- Typical Application Diagram



Block Diagram

The functional blocks of this device are shown below:

Figure 3:
AS1130 Block Diagram



Pin Assignment

Figure 4:
Pin Diagram (Top View)

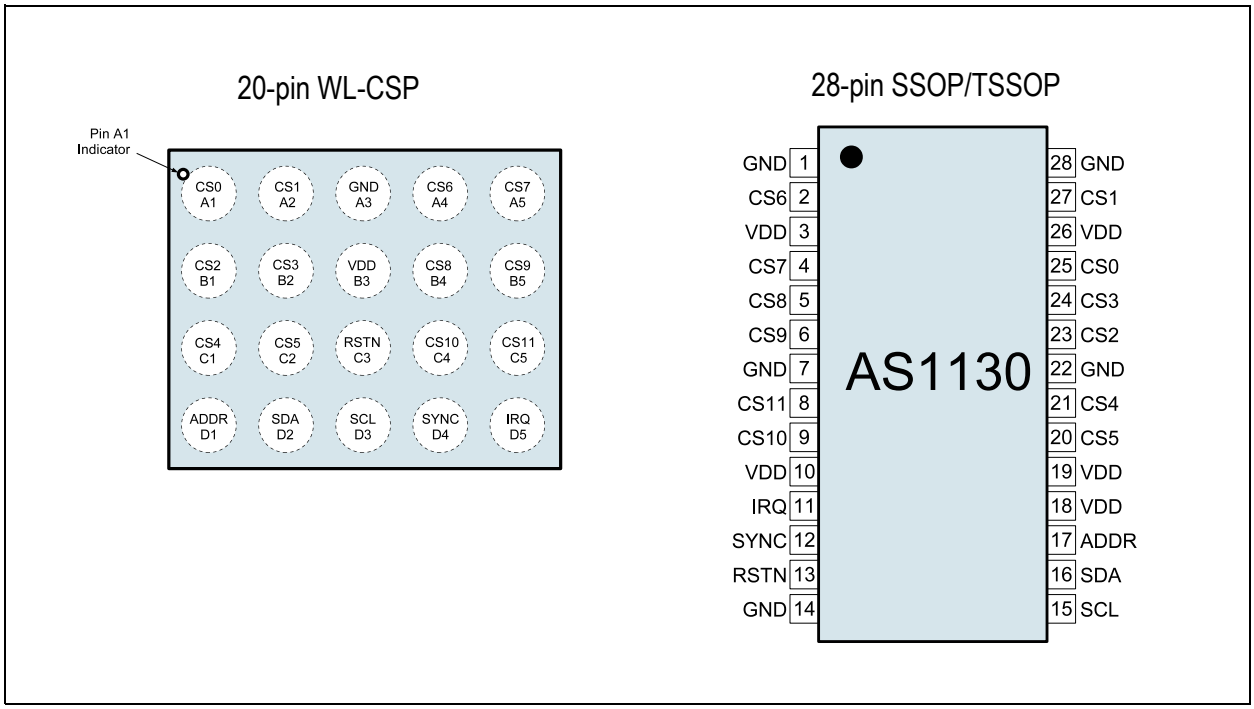


Figure 5:
Pin Description

Pin Number		Pin Name	Description
20-Pin WL-CSP	28-Pin SSOP / TSSOP		
A3	1, 7, 14, 22, 28	GND	**Ground**
C3	13	RSTN	**Reset Input**. Pull this pin to logic low to reset all control registers (set to default values). For normal operation pull this pin to VDD.
D1	17	ADDR	**I²C Address.** Connect to external resistor for I²C address selection. Up to 8 devices can be connected on one bus. See Figure 30
D2	16	SDA	**Serial-Data I/O**. Open drain digital I/O I²C data pin.
D3	15	SCL	**Serial-Clock Input**

Pin Number		Pin Name	Description
20-Pin WL-CSP	28-Pin SSOP / TSSOP		
B3	3, 10, 18, 19, 26	VDD	**Positive Supply Voltage**. Connect to a +2.7V to +5.5V supply. Bypass this pin with 10µF capacitance to GND.
D4	12	SYNC	**Synchronization Clock Input or Output.** The SYNC frequency for Input and Output is 1MHz. For SYNC_OUT the frequency can be reduced to 32kHz.
D5	11	IRQ	**Interrupt Request.** Programmable Open drain digital Output. It can be set via an register after which event (Interface Timeout, POR, CP_ Request, Error Detection, End of Frame or End of Movie) the pin triggers an Interrupt Request.
A1, A2, A4, A5, B1, B2, B4, B5, C1, C2, C4, C5	25, 27, 2, 4, 23, 24, 5, 6, 21, 20, 9, 8	CS0, CS1, CS6, CS7, CS2, CS3, CS8, CS9, CS4, CS5, CS10, CS11	**Sinks and Sources** for 132 LEDs.

Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 6:
Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments	
Electrical Parameters					
V_{DD} to GND	-0.3	7	V		
All other pins to GND	-0.3	7 or V_{DD} + 0.3	V		
Sink Current		500	mA		
Segment Current		100	mA		
Input Current (latch-up immunity)	-100	100	mA	JEDEC 78	
Electrostatic Discharge					
Electrostatic Discharge (human body model)	±2		kV	MIL 883 E method 3015	
Temperature Ranges and Storage Conditions					
Junction Temperature		150	°C		
Storage Temperature Range	-55	125	°C	For 20-Pin WL-CSP	
	-55	150	°C	For 28-pin SSOP/TSSOP	
Package Body Temperature		260	°C	28-pin SSOP/ TSSOP	IPC/JEDEC J-STD-020(1) The lead finish for Pb-free leaded packages is matte tin (100% Sn).
				20-Pin WL-CSP	IPC/JEDEC J-STD-020(1)
Relative Humidity (non-condensing)	5	85	%		
Moisture Sensitivity Level	1			20-Pin WL-CSP	Represents an unlimited floor life time
	3			28-pin SSOP/ TSSOP	Represents a max. floor life time of 168h

Note(s):

1. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices".

Electrical Characteristics

V_{DD} = 2.7V to 5.5V, typ. values are at T_{AMB} = 25°C (unless otherwise specified). All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 7:
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{AMB}	Operating Temperature Range		-40		85	°C
T_J	Operating Junction Temperature Range		-40		125	°C
V_{DD}	Operating Supply Voltage		2.7		5.5	V
I_{DD}	Operating Supply Current	All current sources turned ON, @ V_{DD} = 5.5V		340		mA
		All current sources turned OFF, @ V_{DD} = 5.5V		0.5		
I_{DDSSD}	Software Shutdown Supply Current	All digital inputs at V_{DD} or GND @ V_{DD} = 5.5V		7	15	µA
I_{DDFSD}	Full Shutdown Supply Current	Pin RSTN = 0V, T_{AMB} = 25°C		0.1	1	µA
I_{DIGIT}	Digit Drive Sink Current (drive capability of all sources of one digit[(1)])				360	mA
I_{SEG}	Segment Drive Source Current LED[(2)]	V_{OUT} = 1.8V to V_{DD}-400mV	28	30	32	mA
ΔI_{SEG}	Segment Drive Current Matching LED			1		%
	Device to Device Current Matching LED	V_{OUT} = 1.8V, V_{DD} = 3.3V		1		%
I_{LEAK}	Leakage Output Current	All current sources OFF, V_{OUT} = 0V, V_{DD} = 5.5V, T_{AMB} = 25°C		0.005	0.5	µA
ΔI_{LNR}	Line Regulation	V_{OUT} = 1.8V		0.25		%/V
ΔI_{LDR}	Load Regulation	V_{OUT} = 1.8V to V_{DD}-400mV		0.25		%/V
V_{DSSAT}	Saturation Voltage	Current = 30mA, V_{DD} = 3.3V		200		mV
$R_{DSON(N)}$	Resistance for NMOS			0.3	1	W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Open Detection Level Threshold		V_{DD}- 0.4	V_{DD}- 0.1		V
	Short Detection Level Threshold			770	900	mV
f_{OSC}	Oscillator Frequency		0.9	1	1.1	MHz
$f_{REFRESH}$	Display Scan Rate	12x11 matrix	0.29	0.33	0.36	kHz
t_{RSTN}	Reset Pulse Width Low		500			ns

Note(s):

1. Guaranteed by design.
2. $I_{SEG} = \frac{I_{max} - I_{min}}{I_{max} + I_{min}} \times 100$

Figure 8:
Logic Inputs/Outputs Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IH}, I_{IL}	Logic Input Current	V_{IN} = 0V or V_{DD}	-1		1	µA
V_{IH}	CMOS Logic High Input Voltage		0.7 x V_{DD}			V
V_{IL}	CMOS Logic Low Input Voltage				0.3 x V_{DD}	V
ΔV_I	CMOS Hysteresis Voltage			0.3		V
V_{IH}	Mobile Logic High Input Voltage (1)		1.6			V
V_{IL}	Mobile Logic Low Input Voltage(1)				0.6	V
ΔV_I	Hysteresis Voltage (1)			0.1		V
$V_{OL(SDA)}$	SDA Output Low Voltage	I_{SINK} = 3mA			0.4	V
$V_{OL(IRQ)}$	IRQ Output Low Voltage	I_{SINK} = 3mA			0.4	V
$V_{OL(SYNC\_OUT)}$	Sync Clock Output Low Voltage	I_{SINK} = 1mA			0.4	V
$V_{OH(SYNC\_OUT)}$	Sync Clock Output High Voltage	I_{SOURCE} = 1mA			V_{DD}-0.4	V
	Capacitive Load for Each Bus Line				400	pF

Note(s):

1. Available on request, see Ordering & Contact Information.

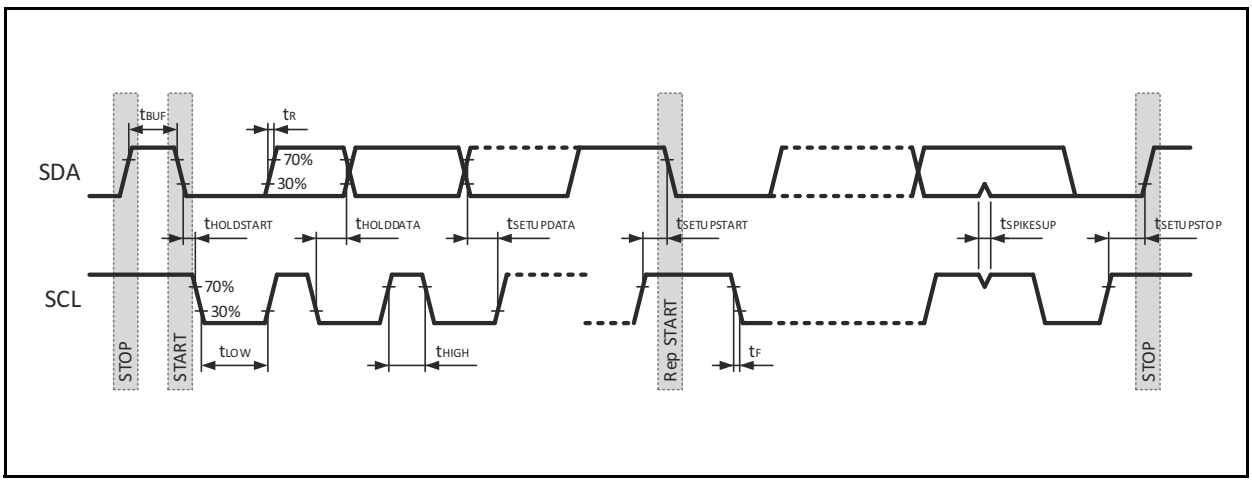
Figure 9:
I²C Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL Frequency		100		1000	kHz
t_{BUF}	Bus Free Time Between STOP and START Conditions		1.3			µs
$t_{HOLDSTART}$	Hold Time for Repeated START Condition		260			ns
t_{LOW}	SCL Low Period		500			ns
t_{HIGH}	SCL High Period		260			ns
$t_{SETUPSTART}$	Setup Time for Repeated START Condition		260			ns
$t_{SETUPDATA}$	Data Setup Time		100			ns
$t_{RISE(SCL)}$	SCL Rise Time				120	ns
$t_{RISE(SCL1)}$	SCL Rise Time after Repeated START Condition and After an ACK Bit				120	ns
$t_{FALL(SCL)}$	SCL Fall Time				120	ns
$t_{RISE(SDA)}$	SDA Rise Time				120	ns
$t_{FALL(SDA)}$	SDA Fall Time				120	ns
$t_{SETUPSTOP}$	STOP Condition Setup Time		260			ns
$t_{SPIKESUP}$	Pulse Width of Spike Suppressed				6	ns

Note(s):

1. The Min / Max values of the Timing Characteristics are guaranteed by design.

Figure 10:
Timing Diagram



Typical Operating Characteristics

Figure 11:
Segment Drive Current vs. Supply Voltage

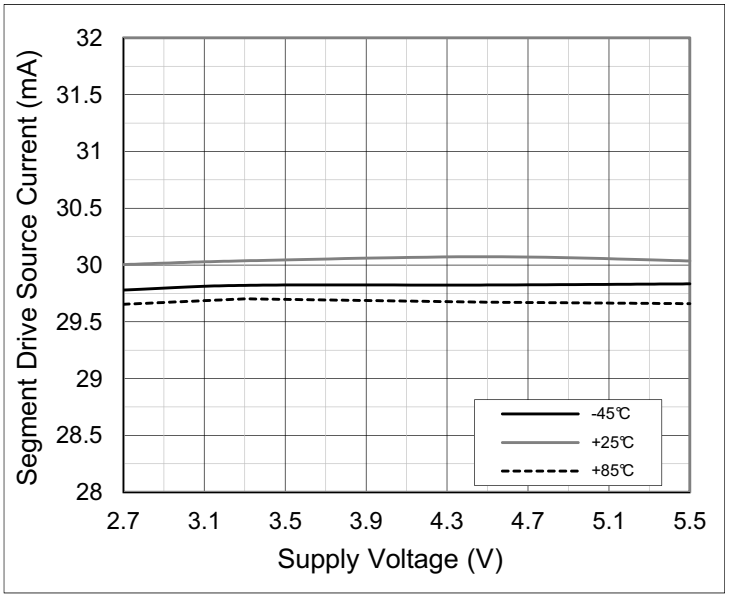


Figure 12:
Segment Drive Current vs. Temperature

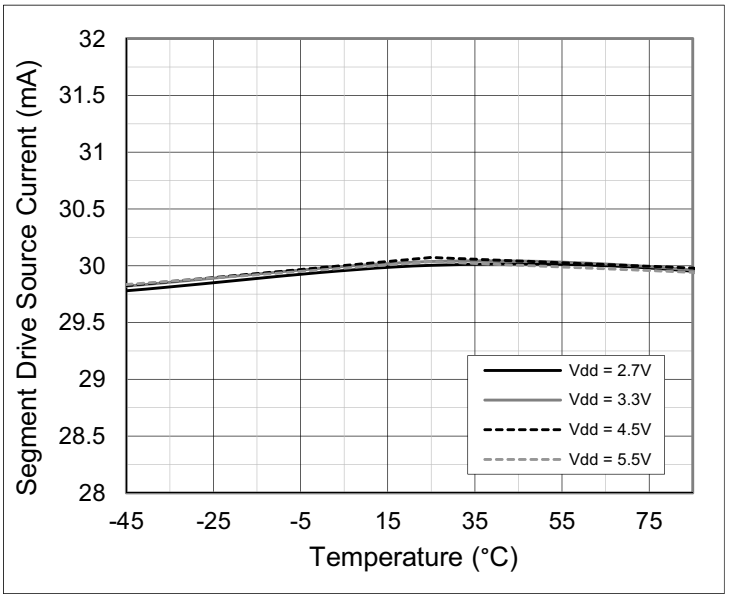


Figure 13:
Segment Drive Current vs. Output Voltage

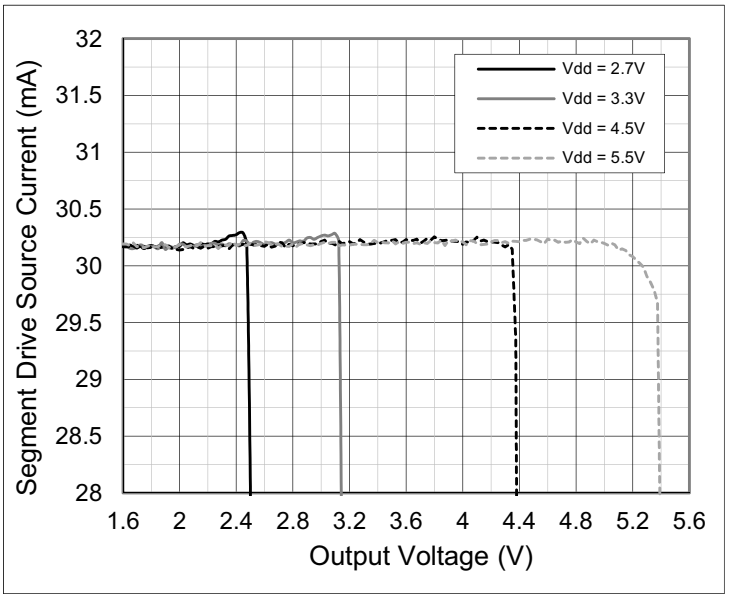


Figure 14:
R_{ONNMOS} vs. Supply Voltage

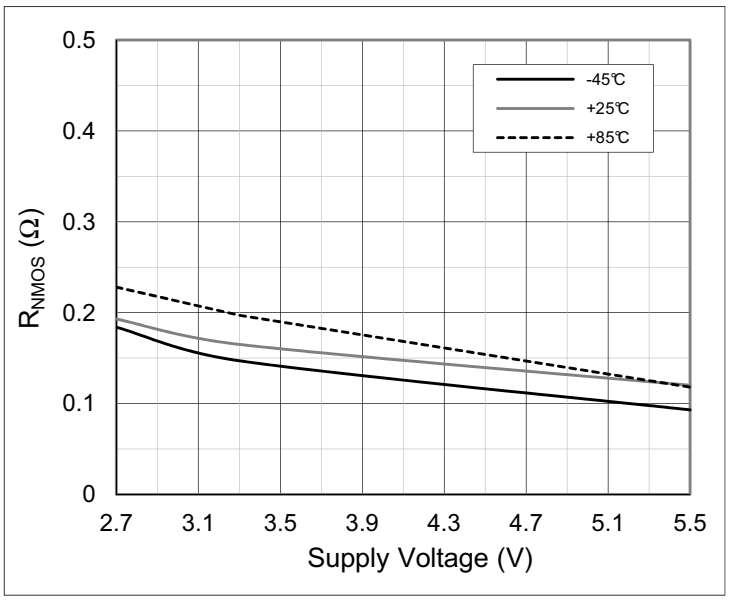


Figure 15:
Open Detection Level vs. Supply Voltage

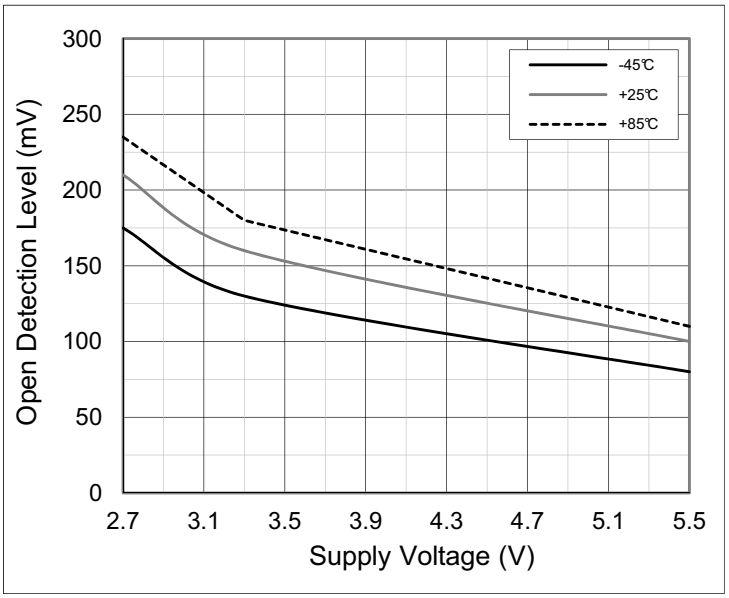


Figure 16:
Short Detection Level vs. Supply Voltage

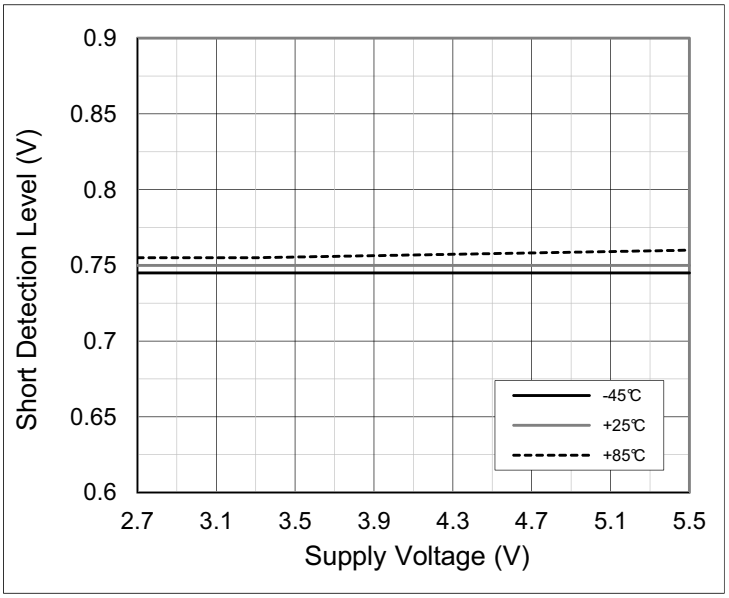


Figure 17:
CMOS Logic Input Levels vs. Supply Voltage

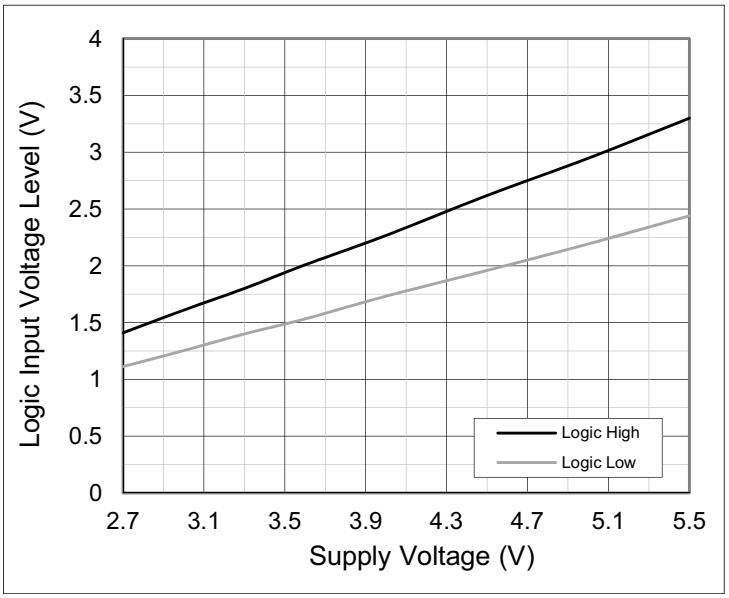


Figure 18:
CMOS Logic Input Levels vs. Temperature

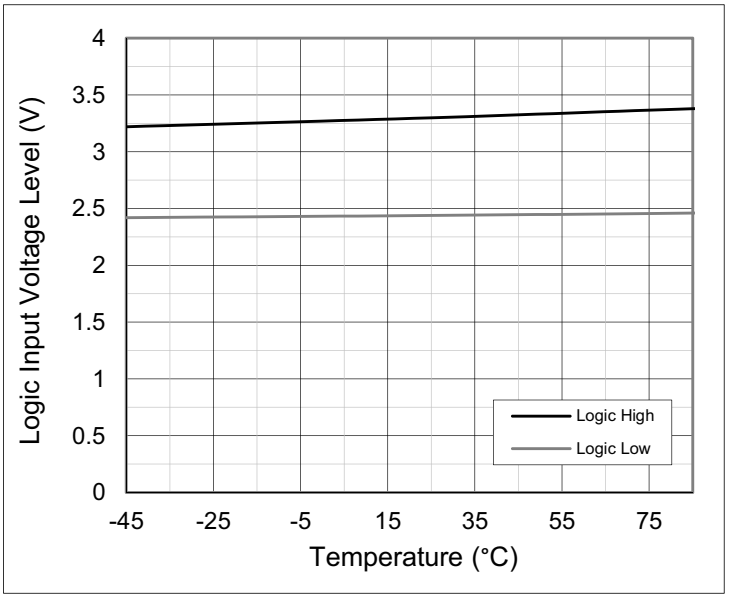


Figure 19:
MOBILE Logic Input Levels vs. Supply Voltage

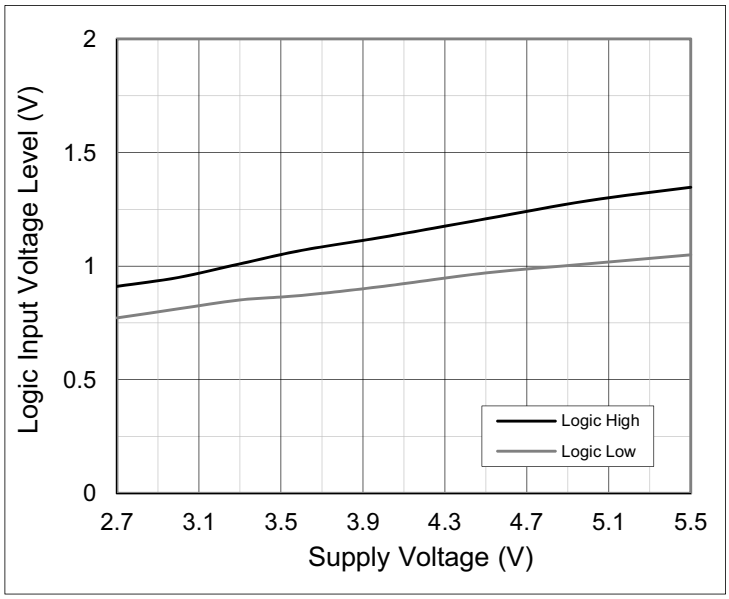


Figure 20:
MOBILE Logic Input Levels vs. Temperature

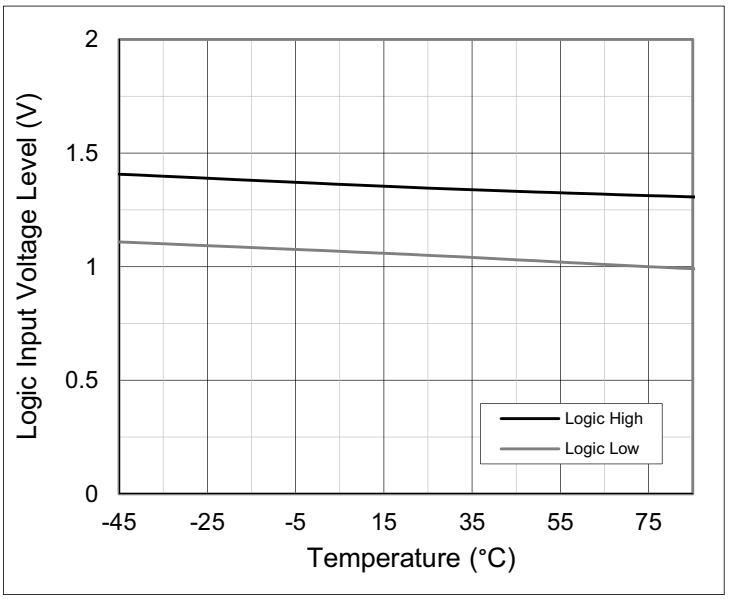


Figure 21:
Oscillator Frequency vs. Supply Voltage

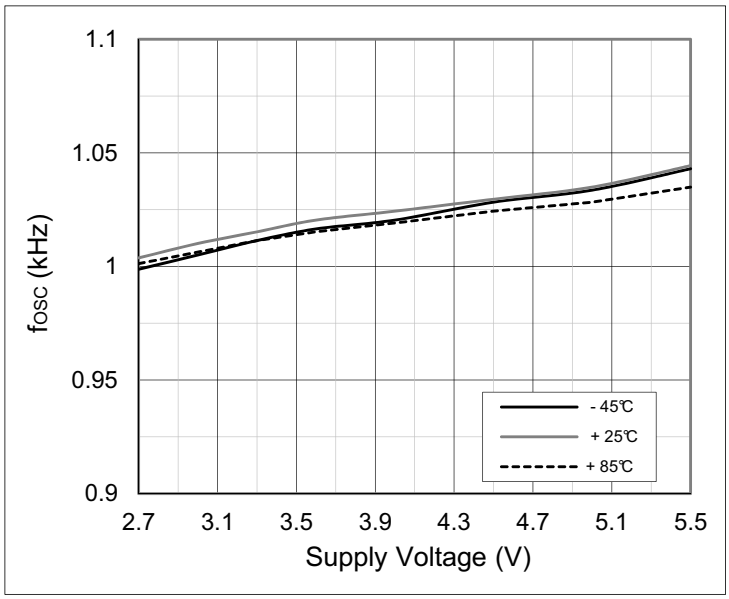
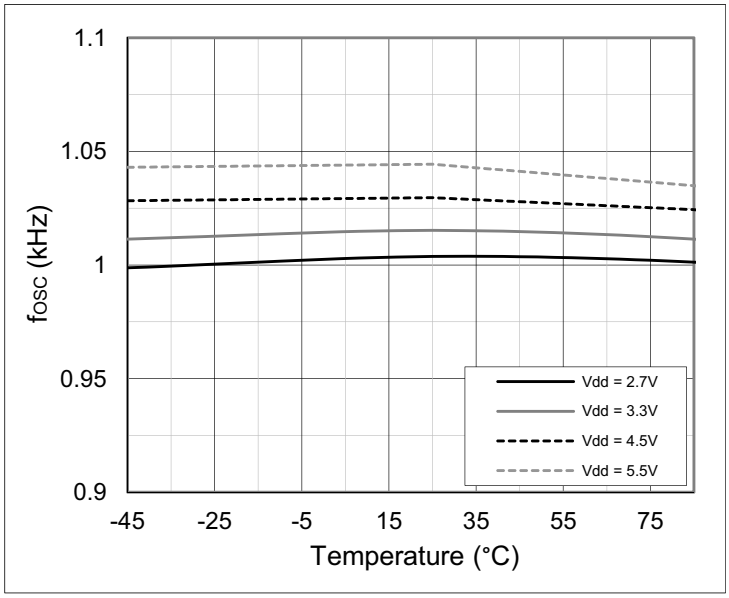


Figure 22:
Oscillator Frequency vs. Temperature



Detailed Description

Cross-Plexing Theorem

The cross-plexing theorem is using the fact that a LED has a forward and backward direction. A LED will only glow if there is a current flowing in forward direction. A parallel LED in backward direction will block the current flow. This effect is used in a cross-plexed matrix of LEDs.

Each CSx pin (CS0 to CS11) can be switched to VDD via the internal current source (“high”), to GND (“low”) or not connected (“highZ”).

The mode of operation which is controlled by an internal state machine looks like following. CS0 is switched to GND and all other CSx pins (CS1 to CS11) are controlled according to the settings in the On/Off Frame and Blink & PWM registers (see Figure 31).

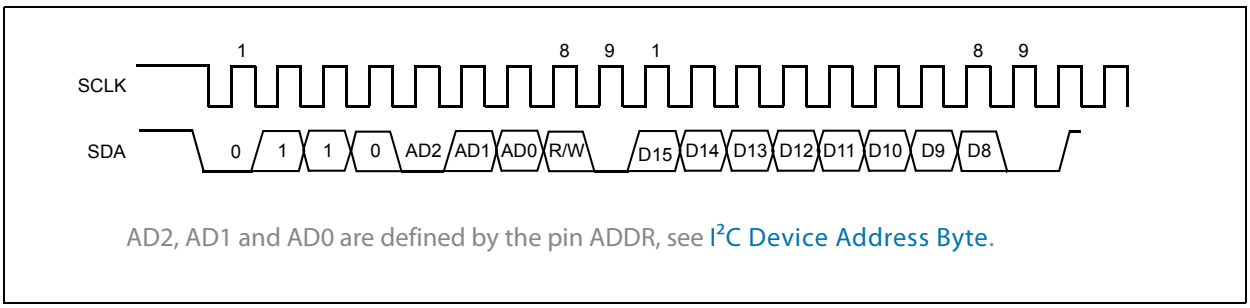
Than CS1 is switched to GND and all other CSx pins (CS0 and CS2 to CS11) are controlled according to the settings in the On/Off Frame and Blink & PWM registers.

In this manner all LEDs in the matrix are scanned and turned on/off depending on the register settings.

I²C Interface

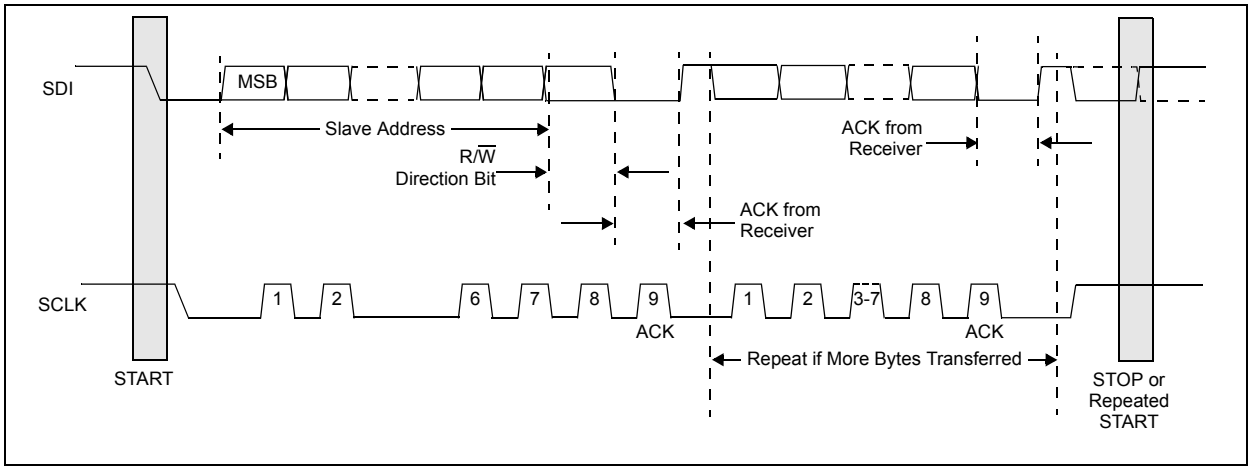
The AS1130 supports the I²C serial bus and data transmission protocol in fast mode at 1MHz. The AS1130 operates as a slave on the I²C bus. The bus must be controlled by a master device that generates the serial clock (SCLK), controls the bus access, and generates the START and STOP conditions. Connections to the bus are made via the open-drain I/O pins SCLK and SDA.

Figure 23:
I²C Interface Initialization



AD2, AD1 and AD0 are defined by the pin ADDR, see I²C Device Address Byte.

Figure 24:
Bus Protocol



The bus protocol (as shown in Figure 24) is defined as:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The bus conditions are defined as:

- **Bus Not Busy**. Data and clock lines remain HIGH.
- **Start Data Transfer**. A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.
- **Stop Data Transfe**r. A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.
- **Data Valid**. The state of the data line represents valid data, when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth-bit. Within the I^2C bus specifications a high-speed mode (3.4MHz clock rate) is defined.

- **Acknowledge**: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.
- Figure 24 details how data transfer is accomplished on the I^2C bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:
  - **Master Transmitter to Slave Receiver**. The first byte transmitted by the master is the slave address, followed by a number of data bytes. The slave returns an acknowledge bit after the slave address and each received byte.
  - **Slave Transmitter to Master Receiver**. The first byte, the slave address, is transmitted by the master. The slave then returns an acknowledge bit. Next, a number of data bytes are transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not-acknowledge is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The AS1130 can operate in the following slave modes:

- **Slave Receiver Mode**. Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
- **Slave Transmitter Mode**. The first byte (the slave address) is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the AS1130 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

Command Byte

The AS1130 operation (see Figure 38) is determined by a command byte (see Figure 25).

Figure 25:
Command Byte

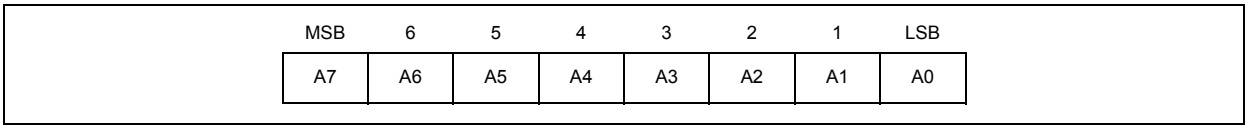


Figure 26:
Command and Single Data Byte Received by AS1130

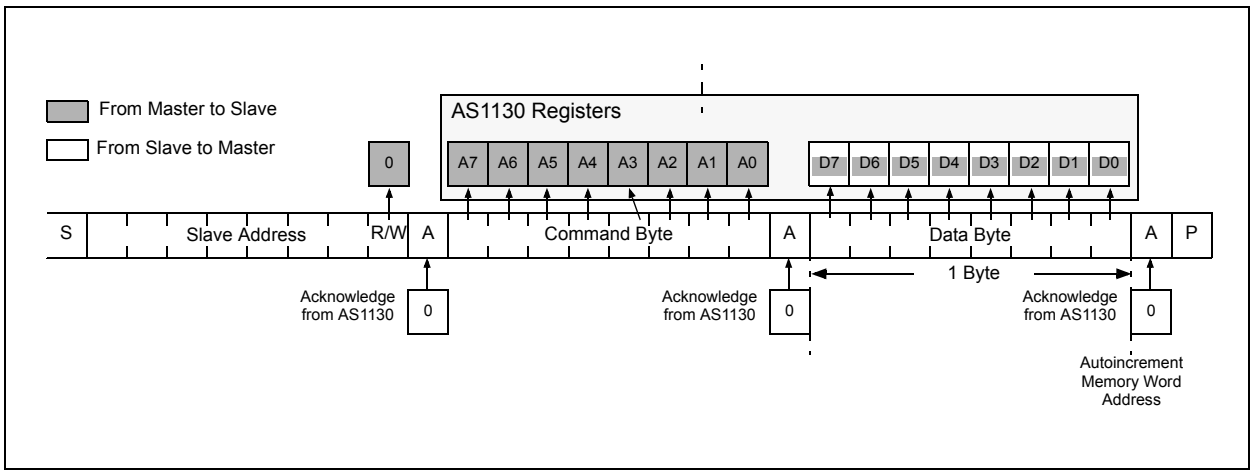


Figure 27:
Setting the Pointer to a Address Register to Select a Data Register for a Read Operation

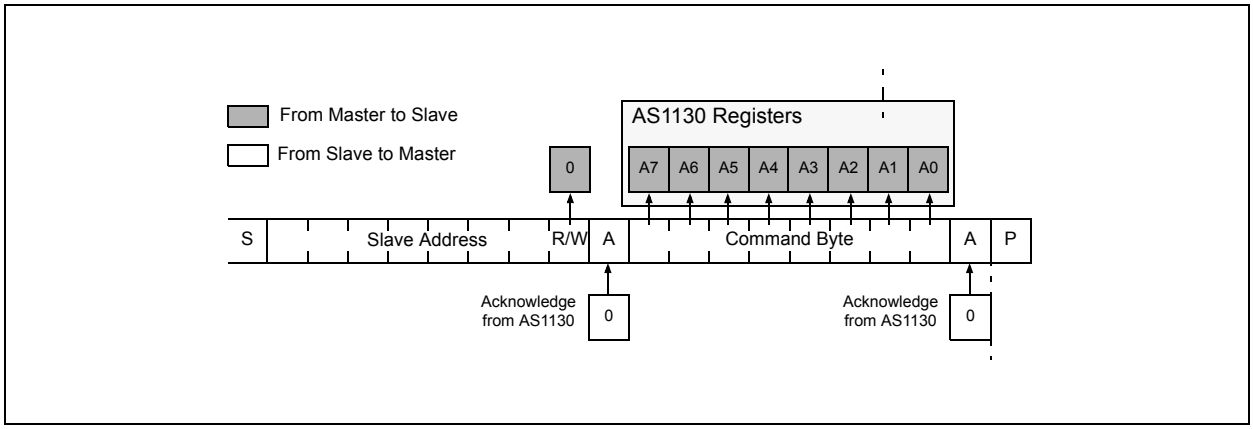
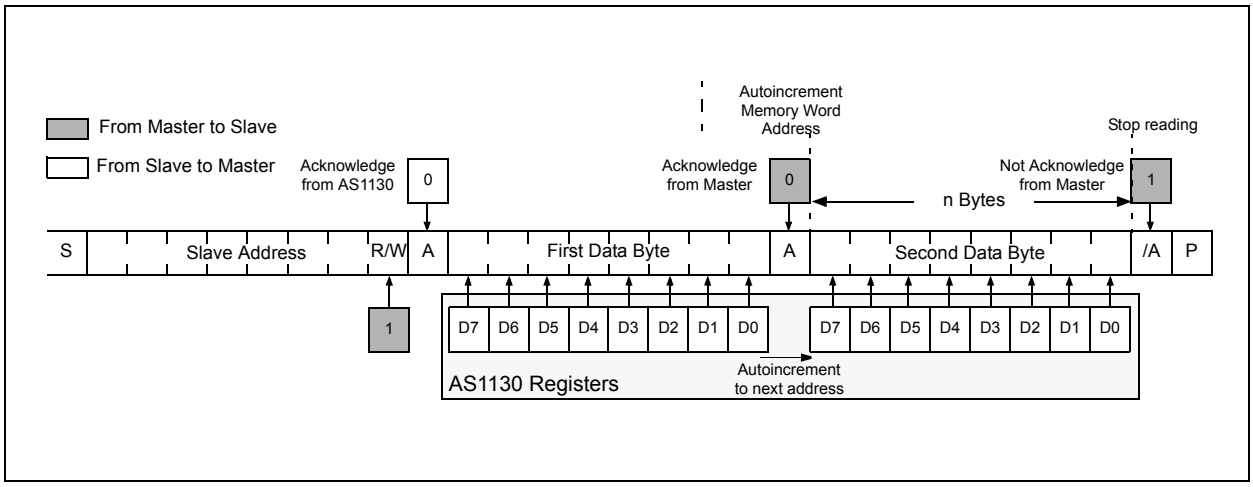


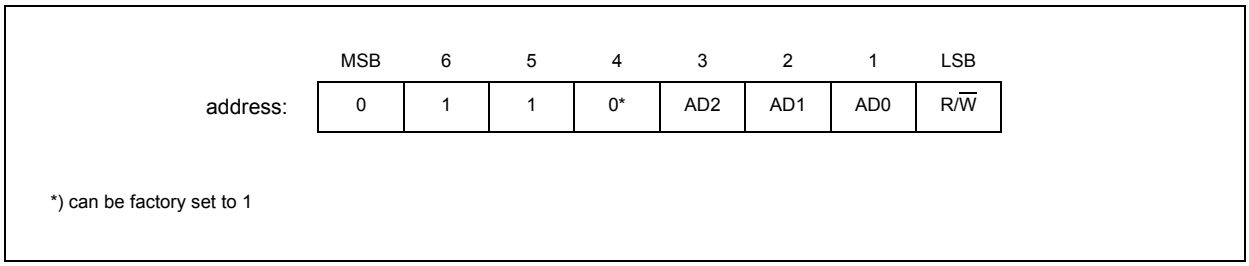
Figure 28:
Reading N Bytes from AS1130



I²C Device Address Byte

The address byte (see Figure 29) is the first byte received following the START condition from the master device.

Figure 29:
I²C Device Address Byte



The bit 1, 2 and 3 of the address byte are defined through the resistor @ the device select pin ADDR (see Figure 30). A maximum of 8 devices with the same pre-set code can be connected on the same bus at one time.

- The last bit of the address byte (R/$\overline{W}$) define the operation to be performed. When set to a 1 a read operation is selected; when set to a 0 a write operation is selected.
- I²C Common address. All devices are responding on the address "0111111" if the function is enabled in the register AS1130 Config Register (0x06).

Following the START condition, the AS1130 monitors the I²C bus, checking the device type identifier being transmitted. Upon receiving the address code, and the R/$\overline{W}$ bit, the slave device outputs an acknowledge signal on the SDA line.

Figure 30:
Device Address

I2C Address				
Bit	**Bit Name**	**Default**	**Access**	**Description**
3:1	i2c_addr	000	R	Defines the I^2C address of one device via an external resistor on pin ADDR **000:** 1MΩ or floating **001:** 470kΩ **010:** 220kΩ **011:** 100kΩ **100:** 47kΩ **101:** 22kΩ **110:** 10kΩ **111:** 4.7kΩ or GND

The pin ADDR is scanned after start up (POR) and defines the address for the device. The device reacts to this address until a hardware reset (low on pin RSTN) is performed or the power-on-reset (POR) triggers again.

Note(s): The internal address decoder needs 5ms to identify the address and to set up the device for this address.

Initial Power-Up

On initial power-up, the AS1130 registers are reset to their default values, the display is blanked, and the device goes into shutdown mode. At this time, all registers should be programmed for normal operation. To bring the device into normal operation the following sequence needs to be performed.

Start-Up Sequence

- Power-up the AS1130 (connect VDD to a source), the devices is in shutdown;
- After 5ms the address of the AS1130 is valid and the first I^2C command can be send.
- Define RAM Configuration; bit mem_conf in the AS1130 Config Register (see Figure 45)
  - On/Off Frames
  - Blink & PWM Sets
  - Dot Correction, if specified
- Define Control Register (see Figure 38)
  - Current Source
  - Display options
  - Display picture / play movie
- To light up the LEDs set the shdn bit to '1' for normal operation mode (see Figure 48).

Shutdown Mode

The AS1130 device features two different shutdown modes. A software shutdown via shutdown register (see Shutdown & Open/Short Register (0x09)) and a hardware shutdown via the RSTN pin.

The software shutdown disables all LEDs and stops the internal operation of the logic. A shutdown mode via the RSTN pin additionally powers down the power-on-reset (POR) of the device. In this shutdown mode the AS1130 consumes only 100nA (typ.).

Register Description

Register Selection

Within this register the access to one of the RAM sections, the Dot Correction or to the Control register is selected. After one section is selected this section is valid as long as an other section is selected.

Figure 31:
Register Selection Address Map

Register Section	Address									Data									Description
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	HEX	D7	D6	D5	D4	D3	D2	D1	D0	
NOP	0xFD	1	1	1	1	1	1	0	1	0x00	0	0	0	0	0	0	0	0	No operation
On/Off Frame 0										0x01	0	0	0	0	0	0	0	1	On/Off information for each frame (up to 36 frames)
On/Off Frame 1										0x02	0	0	0	0	0	0	1	0	
On/Off Frame 2										0x03	0	0	0	0	0	0	1	1	
....										.....									
On/Off Frame 34										0x23	0	0	1	0	0	0	1	1	
On/Off Frame 35										0x24	0	0	1	0	0	1	0	0	
Blink & PWM Set 0										0x40	0	1	0	0	0	0	0	0	Blink & PWM Information Sets (up to 6 sets)
Blink & PWM Set 1										0x41	0	1	0	0	0	0	0	1	
Blink & PWM Set 2										0x42	0	1	0	0	0	0	1	0	
Blink & PWM Set 3										0x43	0	1	0	0	0	0	1	1	
Blink & PWM Set 4										0x44	0	1	0	0	0	1	0	0	
Blink & PWM Set 5										0x45	0	1	0	0	0	1	0	1	
Dot Correction										0x80	1	0	0	0	0	0	0	0	Selection of Dot Correction Register
Control Register										0xC0	1	1	0	0	0	0	0	0	Selection of Control Register

Data Definition of the Single Frames

One frame consists of 2 datasets, the On/Off dataset and the Blink & PWM dataset. Where more On/Off frames can be linked to one PWM set. Depending on the used PWM sets more or less On/Off frames can be stored inside the AS1130 (see Figure 32).

Each On/Off frame needs to define the used Blink & PWM dataset.

Figure 32:
RAM Configuration

RAM Configuration	Blink & PWM Set	On/Off Frame	On/Off Frame with Dot Correction
1	0	35..0	34..0
2	1,0	29..0	28..0
3	2,1,0	23..0	22..0
4	3..0	17..0	16..0
5	4..0	11..0	10..0
6	5..0	5..0	4..0

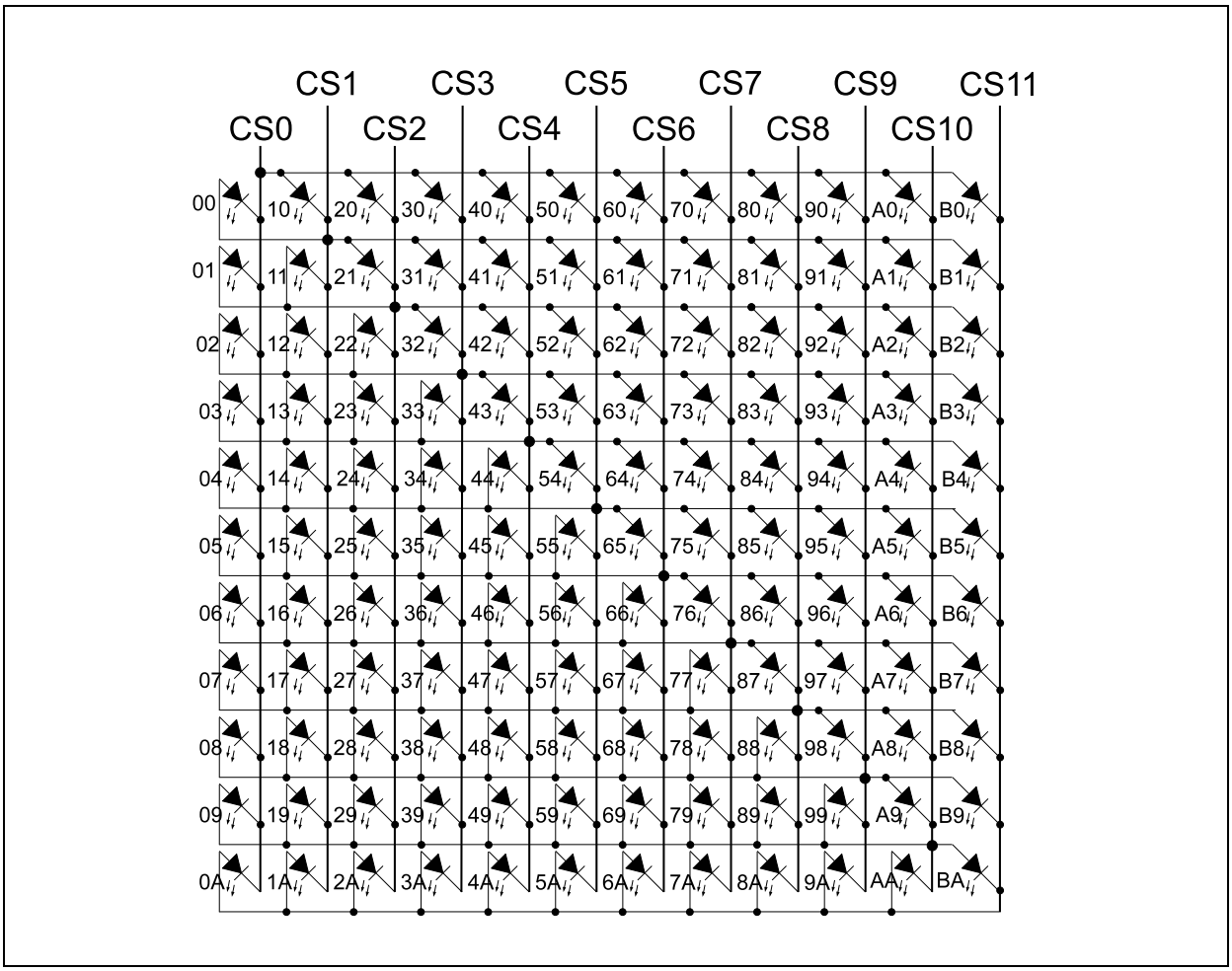
It is necessary to define the RAM configuration before data can be written to the frame datasets. The RAM configuration is defined in the AS1130 config register (see Figure 45) via bit 2:0 and bit 4 for Dot Correction.

Note(s): After a first write of data to the frames, the configuration is locked in the AS1130 config register and can be changed only after a reset of the device. A change of the RAM configuration requires to re-write the frame datasets.

12x11 LED Matrix

The AS1130 is configured to control one big LED matrix.

Figure 33:
AS1130 - Dot Matrix Structure



In Figure 34 it is described which databit represents which LED in the matrix. Per default all databits are '0', meaning no LED is on. A '1' puts the LED on.

Each Current Segment of the LED Matrix consists of 11 LEDs, therefore 2 bytes of data are required for one Current Segment. CS0 is defined by the two bytes with address 0x00 and 0x01 and also includes the address of the used Blink & PWM dataset for this frame.

Figure 34:
LEDs On/Off Frame Register Format

Segment	Address									Data							
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0x00	0	0	0	0	0	0	0	0	LED 07	LED 06	LED 05	LED 04	LED 03	LED 02	LED 01	LED 00
	0x01	0	0	0	0	0	0	0	1	PWM [2]	PWM [1]	PWM [0]	X	X	LED 0A	LED 09	LED 08
1	0x02	0	0	0	0	0	0	1	0	LED 17	LED 16	LED 15	LED 14	LED 13	LED 12	LED 11	LED 10
	0x03	0	0	0	0	0	0	1	1	X	X	X	X	X	LED 1A	LED 19	LED 18
2	0x04	0	0	0	0	0	1	0	0	LED 27	LED 26	LED 25	LED 24	LED 23	LED 22	LED 21	LED 20
	0x05	0	0	0	0	0	1	0	1	X	X	X	X	X	LED 2A	LED 29	LED 28
3	0x06	0	0	0	0	0	1	1	0	LED 37	LED 36	LED 35	LED 34	LED 33	LED 32	LED 31	LED 30
	0x07	0	0	0	0	0	1	1	1	X	X	X	X	X	LED 3A	LED 39	LED 38
4	0x08	0	0	0	0	1	0	0	0	LED 47	LED 46	LED 45	LED 44	LED 43	LED 42	LED 41	LED 40
	0x09	0	0	0	0	1	0	0	1	X	X	X	X	X	LED 4A	LED 49	LED 48

Segment	Address									Data							
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
5	0x0A	0	0	0	0	1	0	1	0	LED 57	LED 56	LED 55	LED 54	LED 53	LED 52	LED 51	LED 50
	0x0B	0	0	0	0	1	0	1	1	X	X	X	X	X	LED 5A	LED 59	LED 58
6	0x0C	0	0	0	0	1	1	0	0	LED 67	LED 66	LED 65	LED 64	LED 63	LED 62	LED 61	LED 60
	0x0D	0	0	0	0	1	1	0	1	X	X	X	X	X	LED 6A	LED 69	LED 68
7	0x0E	0	0	0	0	1	1	1	0	LED 77	LED 76	LED 75	LED 74	LED 73	LED 72	LED 71	LED 70
	0x0F	0	0	0	0	1	1	1	1	X	X	X	X	X	LED 7A	LED 79	LED 78
8	0x10	0	0	0	1	0	0	0	0	LED 87	LED 86	LED 85	LED 84	LED 83	LED 82	LED 81	LED 80
	0x11	0	0	0	1	0	0	0	1	X	X	X	X	X	LED 8A	LED 89	LED 88
9	0x12	0	0	0	1	0	0	1	0	LED 97	LED 96	LED 95	LED 94	LED 93	LED 92	LED 91	LED 90
	0x13	0	0	0	1	0	0	1	1	X	X	X	X	X	LED 9A	LED 99	LED 98
A	0x14	0	0	0	1	0	1	0	0	LED A7	LED A6	LED A5	LED A4	LED A3	LED A2	LED A1	LED A0
	0x15	0	0	0	1	0	1	0	1	X	X	X	X	X	LED AA	LED A9	LED A8

Segment	Address								Data							
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
B	0x16	0	0	0	1	0	1	1	0	LED B7	LED B6	LED B5	LED B4	LED B3	LED B2	LED B1	LED B0
	0x17	0	0	0	1	0	1	1	1	X	X	X	X	X	LED BA	LED B9	LED B8

The Blink & PWM sets contain blink on/off and the digital PWM information for each LED in the matrix. The number of PWM datasets is flexible according to the defined RAM configuration (see Figure 32).

In the blink register (see Figure 35) every single LED can be set to blink. The blink period is set in the display option register (see Display Option Register Format).

Figure 35:
LEDs Blink Frame Register Format

Segment	Address									Data							
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0x00	0	0	0	0	0	0	0	0	LED 07	LED 06	LED 05	LED 04	LED 03	LED 02	LED 01	LED 00
	0x01	0	0	0	0	0	0	0	1	X	X	X	X	X	LED 0A	LED 09	LED 08
1	0x02	0	0	0	0	0	0	1	0	LED 17	LED 16	LED 15	LED 14	LED 13	LED 12	LED 11	LED 10
	0x03	0	0	0	0	0	0	1	1	X	X	X	X	X	LED 1A	LED 19	LED 18

Segment	Address									Data							
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
2	0x04	0	0	0	0	0	1	0	0	LED 27	LED 26	LED 25	LED 24	LED 23	LED 22	LED 21	LED 20
	0x05	0	0	0	0	0	1	0	1	X	X	X	X	X	LED 2A	LED 29	LED 28
3	0x06	0	0	0	0	0	1	1	0	LED 37	LED 36	LED 35	LED 34	LED 33	LED 32	LED 31	LED 30
	0x07	0	0	0	0	0	1	1	1	X	X	X	X	X	LED 3A	LED 39	LED 38
4	0x08	0	0	0	0	1	0	0	0	LED 47	LED 46	LED 45	LED 44	LED 43	LED 42	LED 41	LED 40
	0x09	0	0	0	0	1	0	0	1	X	X	X	X	X	LED 4A	LED 49	LED 48
5	0x0A	0	0	0	0	1	0	1	0	LED 57	LED 56	LED 55	LED 54	LED 53	LED 52	LED 51	LED 50
	0x0B	0	0	0	0	1	0	1	1	X	X	X	X	X	LED 5A	LED 59	LED 58
6	0x0C	0	0	0	0	1	1	0	0	LED 67	LED 66	LED 65	LED 64	LED 63	LED 62	LED 61	LED 60
	0x0D	0	0	0	0	1	1	0	1	X	X	X	X	X	LED 6A	LED 69	LED 68
7	0x0E	0	0	0	0	1	1	1	0	LED 77	LED 76	LED 75	LED 74	LED 73	LED 72	LED 71	LED 70
	0x0F	0	0	0	0	1	1	1	1	X	X	X	X	X	LED 7A	LED 79	LED 78

Segment	Address									Data							
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
8	0x10	0	0	0	1	0	0	0	0	LED 87	LED 86	LED 85	LED 84	LED 83	LED 82	LED 81	LED 80
	0x11	0	0	0	1	0	0	0	1	X	X	X	X	X	LED 8A	LED 89	LED 88
9	0x12	0	0	0	1	0	0	1	0	LED 97	LED 96	LED 95	LED 94	LED 93	LED 92	LED 91	LED 90
	0x13	0	0	0	1	0	0	1	1	X	X	X	X	X	LED 9A	LED 99	LED 98
A	0x14	0	0	0	1	0	1	0	0	LED A7	LED A6	LED A5	LED A4	LED A3	LED A2	LED A1	LED A0
	0x15	0	0	0	1	0	1	0	1	X	X	X	X	X	LED AA	LED A9	LED A8
B	0x16	0	0	0	1	0	1	1	0	LED B7	LED B6	LED B5	LED B4	LED B3	LED B2	LED B1	LED B0
	0x17	0	0	0	1	0	1	1	1	X	X	X	X	X	LED BA	LED B9	LED B8

In the PWM register (see Figure 36) the brightness of every single LED can be set via a 8bit PWM (255 steps).

Figure 36:
LEDs PWM Register Format

Segment		Address									Data							
		HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	LED00	0x18	0	0	0	1	1	0	0	0	255 steps for intensity each single LED							
	LED01	0x19	0	0	0	1	1	0	0	1								
	LED02	0x1A	0	0	0	1	1	0	1	0								
	LED03	0x1B	0	0	0	1	1	0	1	1								
	LED04	0x1C	0	0	0	1	1	1	0	0								
	LED05	0x1D	0	0	0	1	1	1	0	1								
	LED06	0x1E	0	0	0	1	1	1	1	0								
	LED07	0x1F	0	0	0	1	1	1	1	1								
	LED08	0x20	0	0	1	0	0	0	0	0								
	LED09	0x21	0	0	1	0	0	0	0	1								
	LED0A	0x22	0	0	1	0	0	0	1	0								
1	LED10	0x23	0	0	1	0	0	0	1	1	255 steps for intensity each single LED							
	LED11	0x24	0	0	1	0	0	1	0	0								
	LED12	0x25	0	0	1	0	0	1	0	1								
	LED13	0x26	0	0	1	0	0	1	1	0								
	LED14	0x27	0	0	1	0	0	1	1	1								
	LED15	0x28	0	0	1	0	1	0	0	0								
	LED16	0x29	0	0	1	0	1	0	0	1								
	LED17	0x2A	0	0	1	0	1	0	1	0								
	LED18	0x2B	0	0	1	0	1	0	1	1								
	LED19	0x2C	0	0	1	0	1	1	0	0								
	LED1A	0x2D	0	0	1	0	1	1	0	1								

Segment		Address									Data							
		HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
2	LED20	0x2E	0	0	1	0	1	1	1	0	255 steps for intensity each single LED							
	LED21	0x2F	0	0	1	0	1	1	1	1								
	LED22	0x30	0	0	1	1	0	0	0	0								
	LED23	0x31	0	0	1	1	0	0	0	1								
	LED24	0x32	0	0	1	1	0	0	1	0								
	LED25	0x33	0	0	1	1	0	0	1	1								
	LED26	0x34	0	0	1	1	0	1	0	0								
	LED27	0x35	0	0	1	1	0	1	0	1								
	LED28	0x36	0	0	1	1	0	1	1	0								
	LED29	0x37	0	0	1	1	0	1	1	1								
	LED2A	0x38	0	0	1	1	1	0	0	0								
3	LED30	0x39	0	0	1	1	1	0	0	1	255 steps for intensity each single LED							
	LED31	0x3A	0	0	1	1	1	0	1	0								
	LED32	0x3B	0	0	1	1	1	0	1	1								
	LED33	0x3C	0	0	1	1	1	1	0	0								
	LED34	0x3D	0	0	1	1	1	1	0	1								
	LED35	0x3E	0	0	1	1	1	1	1	0								
	LED36	0x3F	0	0	1	1	1	1	1	1								
	LED37	0x40	0	1	0	0	0	0	0	0								
	LED38	0x41	0	1	0	0	0	0	0	1								
	LED39	0x42	0	1	0	0	0	0	1	0								
	LED3A	0x43	0	1	0	0	0	0	1	1								

Segment		Address									Data							
		HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
4	LED40	0x44	0	1	0	0	0	1	0	0	255 steps for intensity each single LED							
	LED41	0x45	0	1	0	0	0	1	0	1								
	LED42	0x46	0	1	0	0	0	1	1	0								
	LED43	0x47	0	1	0	0	0	1	1	1								
	LED44	0x48	0	1	0	0	1	0	0	0								
	LED45	0x49	0	1	0	0	1	0	0	1								
	LED46	0x4A	0	1	0	0	1	0	1	0								
	LED47	0x4B	0	1	0	0	1	0	1	1								
	LED48	0x4C	0	1	0	0	1	1	0	0								
	LED49	0x4D	0	1	0	0	1	1	0	1								
	LED4A	0x4E	0	1	0	0	1	1	1	0								
5	LED50	0x4F	0	1	0	0	1	1	1	1	255 steps for intensity each single LED							
	LED51	0x50	0	1	0	1	0	0	0	0								
	LED52	0x51	0	1	0	1	0	0	0	1								
	LED53	0x52	0	1	0	1	0	0	1	0								
	LED54	0x53	0	1	0	1	0	0	1	1								
	LED55	0x54	0	1	0	1	0	1	0	0								
	LED56	0x55	0	1	0	1	0	1	0	1								
	LED57	0x56	0	1	0	1	0	1	1	0								
	LED58	0x57	0	1	0	1	0	1	1	1								
	LED59	0x58	0	1	0	1	1	0	0	0								
	LED5A	0x59	0	1	0	1	1	0	0	1								
.....																		

Segment		Address									Data							
		HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
A	LEDA0	0x86	1	0	0	0	0	1	1	0	255 steps for intensity each single LED							
	LEDA1	0x87	1	0	0	0	0	1	1	1								
	LEDA2	0x88	1	0	0	0	1	0	0	0								
	LEDA3	0x89	1	0	0	0	1	0	0	1								
	LEDA4	0x8A	1	0	0	0	1	0	1	0								
	LEDA5	0x8B	1	0	0	0	1	0	1	1								
	LEDA6	0x8C	1	0	0	0	1	1	0	0								
	LEDA7	0x8D	1	0	0	0	1	1	0	1								
	LEDA8	0x8E	1	0	0	0	1	1	1	0								
	LEDA9	0x8F	1	0	0	0	1	1	1	1								
	LEDA0	0x90	1	0	0	1	0	0	0	0								
B	LEDB0	0x91	1	0	0	1	0	0	0	1	255 steps for intensity each single LED							
	LEDB1	0x92	1	0	0	1	0	0	1	0								
	LEDB2	0x93	1	0	0	1	0	0	1	1								
	LEDB3	0x94	1	0	0	1	0	1	0	0								
	LEDB4	0x95	1	0	0	1	0	1	0	1								
	LEDB5	0x96	1	0	0	1	0	1	1	0								
	LEDB6	0x97	1	0	0	1	0	1	1	1								
	LEDB7	0x98	1	0	0	1	1	0	0	0								
	LEDB8	0x99	1	0	0	1	1	0	0	1								
	LEDB9	0x9A	1	0	0	1	1	0	1	0								
	LEDBA	0x9B	1	0	0	1	1	0	1	1								

Dot Correction Register

The AS1130 offers a feature to define a correction factor for the analog current for every segment. This correction factor is called Dot Correction and is defined in the Dot Correction register (see Figure 37). The Dot Correction Register is selected via data 128 on addr 253.

Figure 37:
Dot Correction Register Format

Segment	Address									Data							
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0x00	0	0	0	0	0	0	0	0	8 bit Dot Correction							
1	0x01	0	0	0	0	0	0	0	1	8 bit Dot Correction							
2	0x02	0	0	0	0	0	0	1	0	8 bit Dot Correction							
3	0x03	0	0	0	0	0	0	1	1	8 bit Dot Correction							
4	0x04	0	0	0	0	0	1	0	0	8 bit Dot Correction							
5	0x05	0	0	0	0	0	1	0	1	8 bit Dot Correction							
6	0x06	0	0	0	0	0	1	1	0	8 bit Dot Correction							
7	0x07	0	0	0	0	0	1	1	1	8 bit Dot Correction							
8	0x08	0	0	0	0	1	0	0	0	8 bit Dot Correction							
9	0x09	0	0	0	0	1	0	0	1	8 bit Dot Correction							
A	0x0A	0	0	0	0	1	0	1	0	8 bit Dot Correction							
B	0x0B	0	0	0	0	1	0	1	1	8 bit Dot Correction							

Control-Registers

The AS1130 device contains 14 control registers which are listed in Figure 38. All registers are selected using a 8-bit address word, and communication is done via the serial interface. Select the Control Register via the Register Selection (see Figure 31).

The Control Register is selected via data 192 on addr 253.

Figure 38:
Control Register Address Map

Register Name	HEX	Register Address								Register Data
		A7	A6	A5	A4	A3	A2	A1	A0	D7:D0
Picture	0x00	0	0	0	0	0	0	0	0	See Figure 39
Movie	0x01	0	0	0	0	0	0	0	1	See Figure 40
Movie Mode	0x02	0	0	0	0	0	0	1	0	See Figure 41
Frame Time / Scroll	0x03	0	0	0	0	0	0	1	1	See Figure 42
Display Option	0x04	0	0	0	0	0	1	0	0	See Figure 43
Current Source	0x05	0	0	0	0	0	1	0	1	See Figure 44
AS1130 Config	0x06	0	0	0	0	0	1	1	0	See Figure 45
Interrupt Mask	0x07	0	0	0	0	0	1	1	1	See Figure 46
Interrupt Frame Definition	0x08	0	0	0	0	1	0	0	0	See Figure 47
Shutdown & Open/Short	0x09	0	0	0	0	1	0	0	1	See Figure 48
I^2C Interface Monitoring	0x0A	0	0	0	0	1	0	1	0	See Figure 49
CLK Synchronization	0x0B	0	0	0	0	1	0	1	1	See Figure 50
Interrupt Status	0x0E	0	0	0	0	1	1	0	0	See Figure 51
AS1130 Status	0x0F	0	0	0	0	1	1	0	1	See Figure 52
Open LED	0x20	0	0	1	0	0	0	0	0	See Figure 53
	.....									
	0x37	0	0	1	1	0	1	1	1	

Picture Register (0x00)

In this register it must be set if a picture is to display on the LED matrix or not. Also the address of the picture which should be displayed must be set within this register. The default setting of this register is 0x00.

Figure 39:
Picture Register Format

0x00 Picture Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	blink_pic	0	R/W	All LEDs in blink mode during display picture **0:** No blink **1:** All LEDs blink
6	display_pic	0	R/W	Display picture **0:** No picture **1:** Display picture
5:0	pic_addr	000000	R/W	Address of picture **000000:** Frame 0 **000001:** Frame 1 **000010:** Frame 2 **000011:** Frame 3 **000100:** Frame 4 **000101:** Frame 5 ..... **100000:** Frame 32 **100001:** Frame 33 **100010:** Frame 34 **100011:** Frame 35

Note(s):

1. The *display_pic* bit (bit 6 in Picture Register) has lower priority than the *display_movie* bit (bit 6 in Movie Register).

Movie Register (0x01)

In this register it must be set if a movie is to display on the LED matrix or not. Also the address of the first frame in the movie needs be set within this register. The default setting of this register is 0x00.

Figure 40:
Movie Register Format

0x01 Movie Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	blink_movie	0	R/W	All LEDs in blink mode during play movie **0:** No blink **1:** All LEDs blink
6	display_movie	0	R/W	**0:** No movie **1:** Start movie
5:0	movie_addr	000000	R/W	Address of first frame in movie **000000:** Frame 0 **000001:** Frame 1 **000010:** Frame 2 **000011:** Frame 3 **000100:** Frame 4 **000101:** Frame 5 ..... **100000:** Frame 32 **100001:** Frame 33 **100010:** Frame 34 **100011:** Frame 35

Note(s):

1. The *display_movie* bit (bit 6 in Movie Register) has higher priority than the *display_pic* bit (bit 6 in Picture Register).

Movie Mode Register (0x02)

Within this register two movie play options can be set. Per default this register is set to 0x00.

- In scroll mode a movie can stop with the last frame of the movie or scroll endless
- The number of frames to play in a movie

Figure 41:
Movie Mode Register Format

0x02 Movie Mode Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	blink_en	0	R/W	LED blink option(1) **0:** Enabled **1:** Disabled
6	end_last	0	R/W	Defines at which frame a movie stops in scroll mode **0:** Movie ends with 1st frame **1:** Movie ends with last frame
5:0	movie_frames	000000	R/W	Number of frames played in a movie, starting at movie_addr defined in Movie Register **000001:** Play 2 Frames **000010:** Play 3 Frames **000011:** Play 4 Frames **000100:** Play 5 Frames **000101:** Play 6 Frames ..... **100000:** Play 33 Frames **100001:** Play 34 Frames **100010:** Play 35 Frames **100011:** Play 36 Frames

Note(s):

1. Disable blink option overrides any blink definition in PWM data definition or global blink definition in picture register & movie register bit 7.

Frame Time/Scroll Register (0x03)

Every single frame in a movie is displayed for a certain time before the next frame is displayed. This time can be set within this register with 4 bits. The stated values in Figure 42 are typical values.

Also the scroll options are set within this register. Per default this register is set to 0x00.

Figure 42:
Frame Time/Scroll Register Format

0x03 Frame Time/Scroll Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	frame_fad	0	R/W	Fade frame option (not available in 5 LED block configuration) **0:** No fading **1:** Fading of a frame
6	scroll_dir	0	R/W	Scroll Direction **0:** Scroll to right **1:** Scroll to left
5	block_size	0	R/W	Define block size for scrolling **0:** Scroll in full matrix **1:** Scroll in 5 LED blocks (current sources split in 2 sections, see Scroll Function)
4	Enable Scrolling	0	R/W	Scroll digits at play movie **0:** No scrolling **1:** Scrolling digits at play movie
3:0	frame_delay	0000	R/W	Delay between frame change in a movie **0000:** Play frame only one time **0001:** 32.5ms **0010:** 65ms **0011:** 97.5ms **0100:** 130ms **0101:** 162.5ms **0110:** 195ms **0111:** 227.5ms **1000:** 260ms **1001:** 292.5ms **1010:** 325ms **1011:** 357.5ms **1100:** 390ms **1101:** 422.5ms **1110:** 455ms **1111:** 487.5ms

Display Option Register (0x04)

In this register the number of loops in a movie are defined. With the scan-limit it can be controlled how many digits are displayed in each matrix. When all 12 digits in the matrix are displayed, the display scan rate is 430Hz (typ.). If the number of digits to display is reduced, the update frequency is increased. Per default this register is set to 0x20.

Figure 43:
Display Option Register Format

0x04 Display Option Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	loops	001	R/W	Number of loops played in one movie **000:** Not valid **001:** 1 loop **010:** 2 loops **011:** 3 loops **100:** 4 loops **101:** 5 loops **110:** 6 loops **111:** play movie endless (needs to be reset to 0-6 to stop movie); for scroll endless set bit end_last = '0'
4	blink_freq	0	R/W	Blink period **0:** 1.5s **1:** 3s
3:0	scan_limit	0000	R/W	Number of displayed segments in one frame (scan-limit) **0000:** CS0 **0001:** CS0 to CS1 **0010:** CS0 to CS2 **0011:** CS0 to CS3 **0100:** CS0 to CS4 **0101:** CS0 to CS5 **0110:** CS0 to CS6 **0111:** CS0 to CS7 **1000:** CS0 to CS8 **1001:** CS0 to CS9 **1010:** CS0 to CS10 **1011:** CS0 to CS11

Note(s):

1. To stop a movie in *play endless* mode, bits D7:D5 have to be set to a value between 000 to 110.

Current Source Register (0x05)

Within this registers the current for every single LED can be set from 0mA to 30mA in 255 steps (8 bits). Per default this register is set to 0x00.

Figure 44:
Current Source Register Format

0x05 Current Source Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	current	00000000	R/W	**00000000:** 0mA **11111111:** 30mA

AS1130 Config Register (0x06)

Per default this register is set to 0x00.

Figure 45:
AS1130 Config Register Format

0x06 AS1130 Config Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	low_vdd_rst	0	R/W	**0:** At the end of a movie or a display picture the "low_VDD" flag is not changed **1:** At the end of a movie or a display picture, the "low_VDD" flag is set to "0"
6	low_vdd_stat	0	R/W	This bit indicates the supply status **0:** If low_VDD is detected, the Interrupt Status Register will be updated accordingly and pin IRQ is triggered. **1:** The low_VDD bit is directly mapped to the pin IRQ. This can be used to control an external DC/DC Converter or Charge Pump. In this case pin IRQ cannot be used for interrupt functionality, the Interrupt Status Register will be updated accordingly.
5	led_error_correction	0	R/W	This bit defines the LED open handling **0:** Open LEDs which are detected at LED open test, are NOT disabled **1:** Open LEDs which are detected at LED open test, are disabled
4	dot_corr	0	R/W	Analog current DotCorrection(1) **0:** Disabled **1:** Enabled

0x06 AS1130 Config Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3	common_addr	0	R/W	I^2C Common Address **0:** Disabled **1:** Enabled (all AS1130 are reacting on the same address "0111111")
2:0	mem_conf	000	R/W	Define Memory Configuration(1) (see RAM Configuration) **000:** Invalid Configuration (default value) **001:** RAM Configuration 1 **010:** RAM Configuration 2 **011:** RAM Configuration 3 **100:** RAM Configuration 4 **101:** RAM Configuration 5 **110:** RAM Configuration 6

Note(s):

1. This configuration is locked after the first write access to ON/OFF, PWM od DotCorrection data section. Unlock can be performed only by a reset of the device.

Interrupt Mask Register (0x07)

Per default this register is set to 0x20.

Figure 46:
Interrupt Mask Register Format

0x07 Interrupt Mask Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	selected_pic	0	R/W	IRQ pin triggers if defined frame is displayed (see Interrupt Frame Definition Register (0x08)) **0:** Disabled **1:** Enabled
6	watchdog	0	R/W	IRQ pin triggers if the I^2C watchdog triggers **0:** Disabled **1:** Enabled
5	por	1	R/W	IRQ pin triggers if POR is active **0:** Disabled **1:** Enabled
4	overtemp	0	R/W	IRQ pin triggers if the overtemperature limit is reached **0:** Disabled **1:** Enabled
3	low_vdd	0	R/W	IRQ pin triggers if V_{DD} is too low for used LEDs (low_VDD flag) **0:** Disabled **1:** Enabled

0x07 Interrupt Mask Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2	open_err	0	R/W	IRQ pin triggers if an error on the open test occurs **0:** Disabled **1:** Enabled
1	short_err	0	R/W	IRQ pin triggers if an error on the short test occurs **0:** Disabled **1:** Enabled
0	movie_fin	0	R/W	IRQ pin triggers if a movie is finished **0:** Disabled **1:** Enabled

Interrupt Frame Definition Register (0x08)

Per default this register is set to 0x3F.

Figure 47:
Interrupt Frame Definition Register Format

0x08 Interrupt Frame Definition Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	-	00	n/a	
5:0	last_frame	111111	R/W	After this frame is displayed the last time (depending on the number of loops played in a movie) an interrupt will be triggered. **000000:** Frame 0 **000001:** Frame 1 **000010:** Frame 2 **000011:** Frame 3 **000100:** Frame 4 **000101:** Frame 5 ..... **100000:** Frame 32 **100001:** Frame 33 **100010:** Frame 34 **100011:** Frame 35

Shutdown & Open/Short Register (0x09)

Per default this register is set to 0x02.

Figure 48:
Shutdown & Open/Short Register Format

0x09 Shutdown & Open/Short Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	-	000	n/a	
4	test_all	0	R/W	The LED open/short test is performed on all LED locations **0:** Disabled (unassembled or disabled LEDs will be detected as open) **1:** Enabled (unassembled LEDs will be detected as open)
3	auto_test	0	R/W	The automatic LED open/short test is started when bit display_pic (0x00) or bit display_movie (0x01) is set to "1" **0:** Disabled **1:** Enabled
2	manual_test	0	R/W	The manual LED open/short test is started after the update of Reg0x09 **0:** Disabled **1:** Enabled
1	init	1	R/W	**0:** Initialise control logic (internal state machine is reset again) **1:** Normal operation
0	shdn	0	R/W	**0:** Device is in shutdown mode (outputs are turned off, internal state machine stops) **1:** Normal operation

The scan limit (0x04) defines also the number of segments for the open/short detection.

I²C Interface Monitoring Register (0x0A)

This register is used to monitor the activity on the I²C bus. If a deadlock situation occurs (e.g. the bus SDA pin is pulled to low and no communication is possible) the chip will reset the I²C interface and the master is able to start the communication again.

The time window for the reset of the interface of the AS1130 can be set via 7 bits from 256µs to 33ms. The default setting of this register is 0xFF.

Figure 49:
I²C Interface Monitoring Register Format

0x0A I²C Interface Monitoring Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	-	1	n/a	
6:1	Timeout window	11111	R/W	Definition of the Timeout window (0 to 127 => 1 to 128 x 256µs) **0000000:** 256µs **1111111:** 32.7ms
0	i2c_monitor	1	R/W	**0:** I²C monitoring off **1:** I²C monitoring on

CLK Synchronization Register (0x0B)

The default setting of this register is 0x00.

Figure 50:
CLK Synchronization Register Format

0x0B CLK Synchronization Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	-	0000	n/a	
3:2	clk_out	00	R/W	Adjustable clock out frequency **00:** 1MHz **01:** 500kHz **10:** 125kHz **11:** 32kHz
1	sync_out	0	R/W	The internal oscillator is used as system-clk. The selected clk frequency is available on pin D4 for synchronization. (Output)(1) **0:** Disabled **1:** Enabled

0x0B CLK Synchronization Register				
Bit	Bit Name	Default	Access	Bit Description
0	sync_in	0	R/W	The internal oscillator is disabled. Pin D4 is used as clk input for system-clk.(1) **0:** disabled **1:** enabled

Note(s):

1. CLK synchronization is done via the SYNC pin. Only one option can be activated (Input or Output).

Interrupt Status Register (0x0E)

This is a read only register. Within this register the cause of an interrupt can be read out. After power up or a reset the default setting of this register is 0x20. A read out command will set this register to default and the IRQ pin will be released again.

Figure 51:
Interrupt Status Register Format

0x0E Interrupt Status Register				
Bit	Bit Name	Default	Access	Bit Description
7	frame_int	0	R	**0:** No interrupt **1:** Defined Frame is displayed (see Interrupt Frame Definition Register (0x08))
6	i2c_int	0	R	**0:** No interrupt **1:** I^2C watchdog reports a deadlock on the interface
5	por_int	1	R	**0:** No interrupt **1:** POR was triggered
4	overtemp_int	0	R	**0:** No interrupt **1:** Overtemperature limit is reached
3	low_vdd_int	0	R	**0:** No interrupt **1:** V_{DD} is too low to drive requested current through the LEDs
2	open_int	0	R	**0:** No interrupt **1:** Error on open test
1	short_int	0	R	**0:** No interrupt **1:** Error on short test
0	movie_int	0	R	0: No interrupt 1: Play movie is finished

AS1130 Status Register (0x0F)

This is a read only register. From this register the actual status of the AS1130 can be read out. The default setting of this register is 0x00.

Figure 52:
AS1130 Status Register Format

0x0F AS1130 Status Register				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	frame_on	000000	R	Actual displayed frame **000000:** Frame 0 **000001:** Frame 1 **000010:** Frame 2 **000011:** Frame 3 **000100:** Frame 4 **000101:** Frame 5 ..... **100000:** Frame 32 **100001:** Frame 33 **100010:** Frame 34 **100011:** Frame 35
1	movie_on	0	R	**0:** No movie **1:** Movie playing
0	test_on	0	R	**0:** No test is running **1:** Open/short test ongoing

AS1130 Open LED Register (0x20 to 0x37)

This is a read only register. From this register the LED's which failed with an open error can be read out. A '1' indicates LED okay, a '0' stands for LED open. If a LED, which is physically not connected to the device is tested, the Open LED test will return a '0'.

Figure 53:
Open LED Register Format

Segment	Address									Data							
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0x20	0	0	1	0	0	0	0	0	LED 07	LED 06	LED 05	LED 04	LED 03	LED 02	LED 01	LED 00
	0x21	0	0	1	0	0	0	0	1	0	0	0	0	0	LED 0A	LED 09	LED 08
1	0x22	0	0	1	0	0	0	1	0	LED 17	LED 16	LED 15	LED 14	LED 13	LED 12	LED 11	LED 10
	0x23	0	0	1	0	0	0	1	1	0	0	0	0	0	LED 1A	LED 19	LED 18
2	0x24	0	0	1	0	0	1	0	0	LED 27	LED 26	LED 25	LED 24	LED 23	LED 22	LED 21	LED 20
	0x25	0	0	1	0	0	1	0	1	0	0	0	0	0	LED 2A	LED 29	LED 28
3	0x26	0	0	1	0	0	1	1	0	LED 37	LED 36	LED 35	LED 34	LED 33	LED 32	LED 31	LED 30
	0x27	0	0	1	0	0	1	1	1	0	0	0	0	0	LED 3A	LED 39	LED 38

Segment	Address									Data							
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
4	0x28	0	0	1	0	1	0	0	0	LED 47	LED 46	LED 45	LED 44	LED 43	LED 42	LED 41	LED 40
	0x29	0	0	1	0	1	0	0	1	0	0	0	0	0	LED 4A	LED 49	LED 48
5	0x2A	0	0	1	0	1	0	1	0	LED 57	LED 56	LED 55	LED 54	LED 53	LED 52	LED 51	LED 50
	0x2B	0	0	1	0	1	0	1	1	0	0	0	0	0	LED 5A	LED 59	LED 58
6	0x2C	0	0	1	0	1	1	0	0	LED 67	LED 66	LED 65	LED 64	LED 63	LED 62	LED 61	LED 60
	0x2D	0	0	1	0	1	1	0	1	0	0	0	0	0	LED 6A	LED 69	LED 68
7	0x2E	0	0	1	0	1	1	1	0	LED 77	LED 76	LED 75	LED 74	LED 73	LED 72	LED 71	LED 70
	0x2F	0	0	1	0	1	1	1	1	0	0	0	0	0	LED 7A	LED 79	LED 78
8	0x30	0	0	1	1	0	0	0	0	LED 87	LED 86	LED 85	LED 84	LED 83	LED 82	LED 81	LED 80
	0x31	0	0	1	1	0	0	0	1	0	0	0	0	0	LED 8A	LED 89	LED 88
9	0x32	0	0	1	1	0	0	1	0	LED 97	LED 96	LED 95	LED 94	LED 93	LED 92	LED 91	LED 90
	0x33	0	0	1	1	0	0	1	1	0	0	0	0	0	LED 9A	LED 99	LED 98

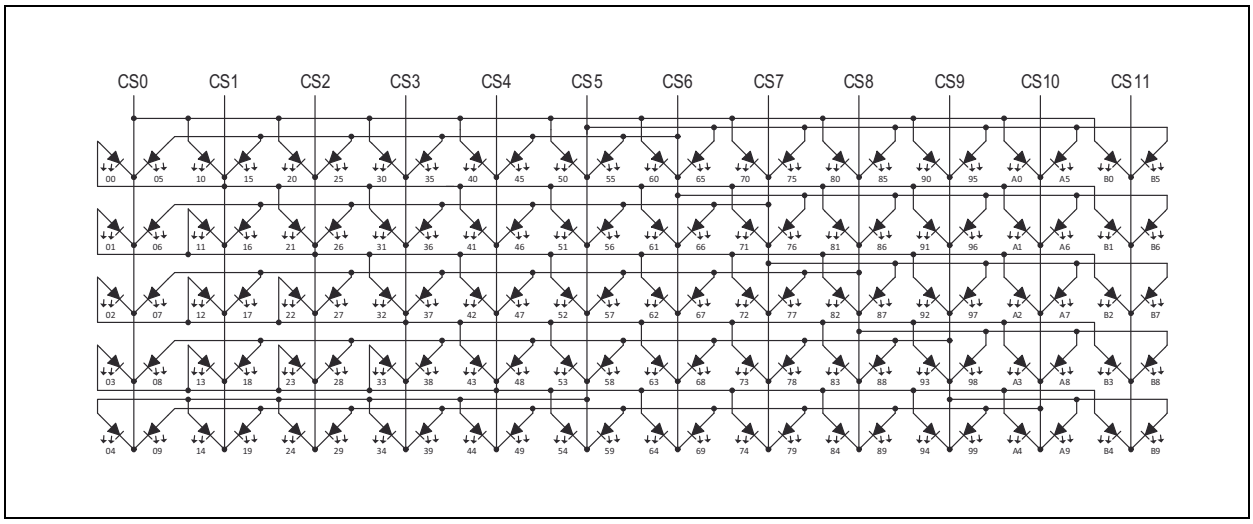
Segment	Address									Data							
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
A	0x34	0	0	1	1	0	1	0	0	LED A7	LED A6	LED A5	LED A4	LED A3	LED A2	LED A1	LED A0
	0x35	0	0	1	1	0	1	0	1	0	0	0	0	0	LED AA	LED A9	LED A8
B	0x36	0	0	1	1	0	1	1	0	LED B7	LED B6	LED B5	LED B4	LED B3	LED B2	LED B1	LED B0
	0x37	0	0	1	1	0	1	1	1	0	0	0	0	0	LED BA	LED B9	LED B8

Typical Application

Scroll Function

The AS1130 offers a feature for scrolling a picture through the matrix without the need of communication via a µP. The scrolling can be done in the whole matrix (12x11) or optimized for a ticker in a 5x24 matrix (see Figure 54).

Figure 54:
LED Configuration for 5LED Block Scroll Function



In the movie display mode the frame is shown in the matrix at once. On the contrary in the scroll function the frame is shifted through the matrix segment after segment (CS0 to CS1 to CS2 to CS3...).

Figure 55:
Scrolling

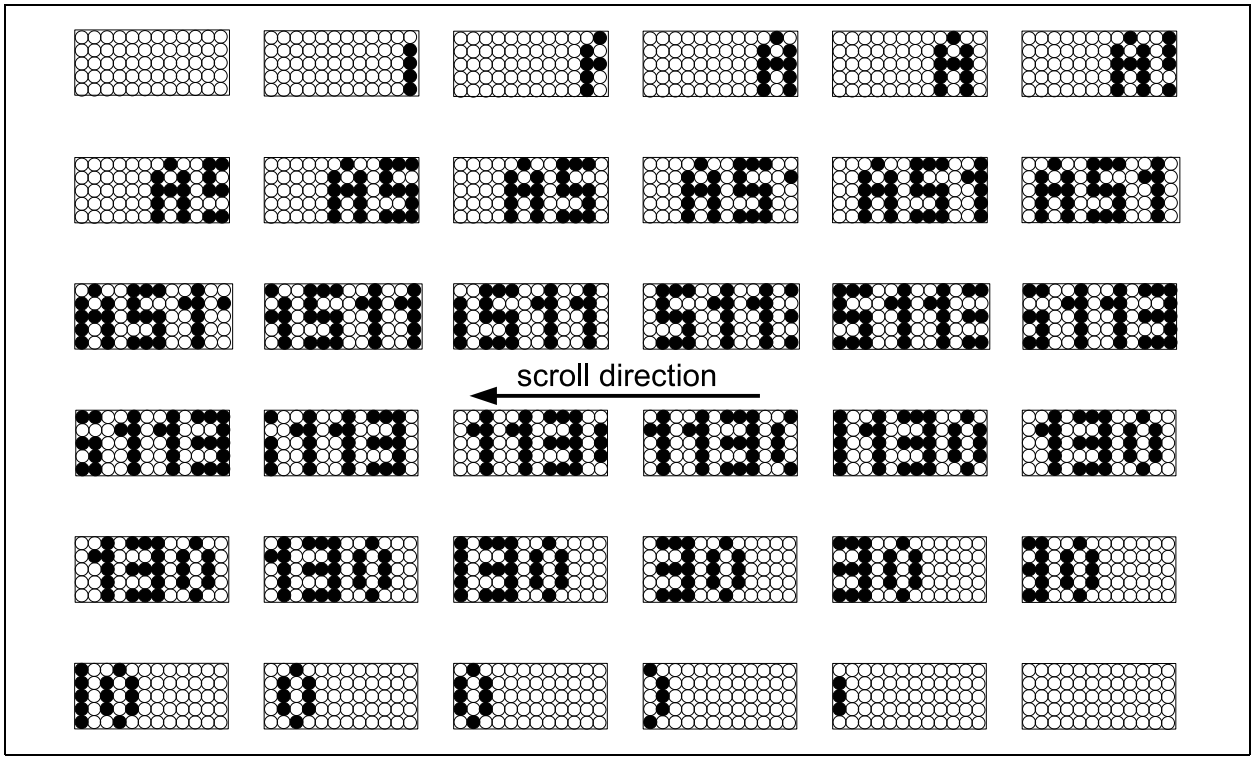
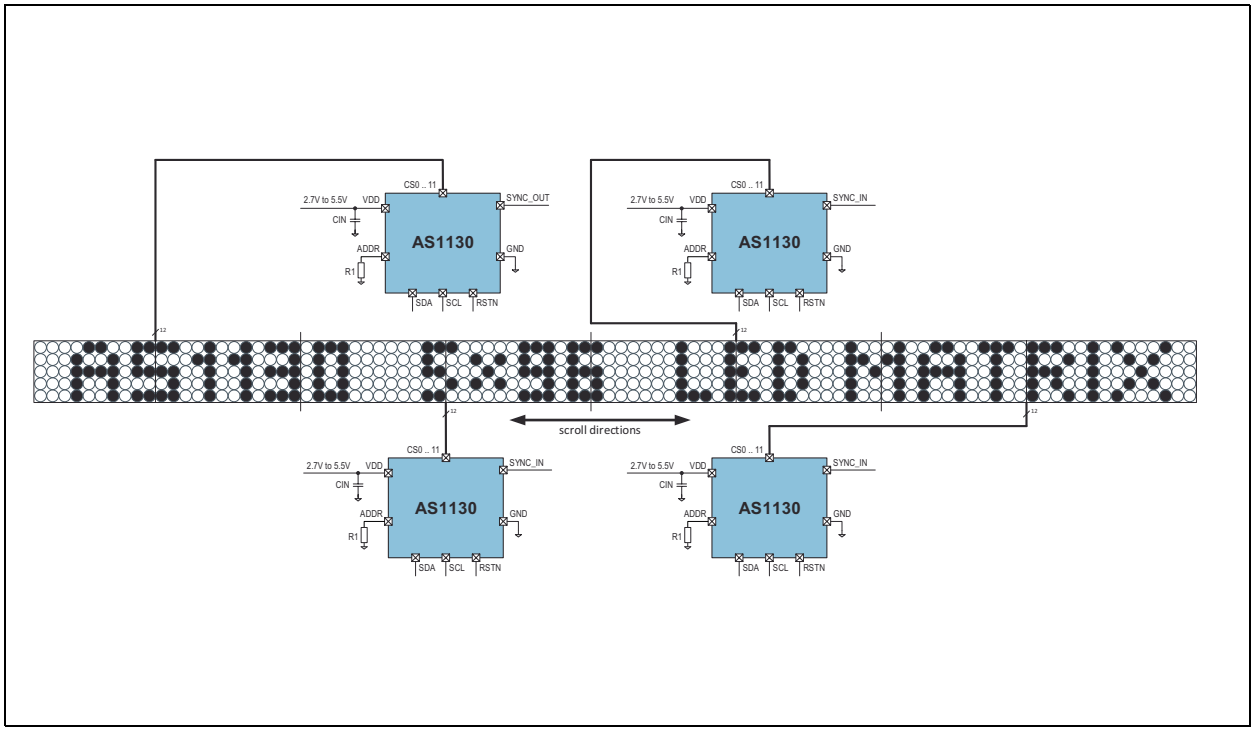


Figure 56:
Ticker Application with 5x96 LED Matrix



LED Current Calculation

The current through a LED in the matrix is set via three registers (Current Source Register, Dot Correction and PWM). The resulting current through the single LED can be calculated as shown in the following.

First it is necessary to calculate the time how long one LED will be ON.

(EQ1)

$$t_{LEDon} = \frac{PWM}{f_{OSC}}$$

Where:

t_{LEDon}: Time where the LED is ON

PWM:. Value set in the register (0 - 256), see Figure 36

f_{OSC}: Frequency set in the CLK Synchronization Register, see Figure 50.

The refresh rate is defined by the scan-limit and f_{OSC}.

(EQ2)

$$t_{REFRESH} = \frac{(scanlimit + 1) \times 256}{f_{OSC}}$$

Where:

$t_{REFRESH}$: Time needed to refresh the matrix scan-limit. is set via the Display Option Register (0 - 11), see Figure 43

f_{OSC}: frequency set in the CLK Synchronization Register, see Figure 50

With the LED on-time and the refresh rate an average LED ON factor can be calculated.

(EQ3)

$$LEDon_{avg} = \frac{t_{LEDon}}{t_{REFRESH}} = \frac{PWM}{(scanlimit + 1) \times 256}$$

The resulting current is then the Segment Current (set in the Current Source Register) times the average LED ON factor.

(EQ4)

$$I_{LEDavg} = I_{SEG} \times LEDon_{avg} = I_{SEG} \times \frac{PWM}{(scanlimit + 1) \times 256}$$

Where:

I_{SEG}: Segment Current set via register Figure 44

Example:

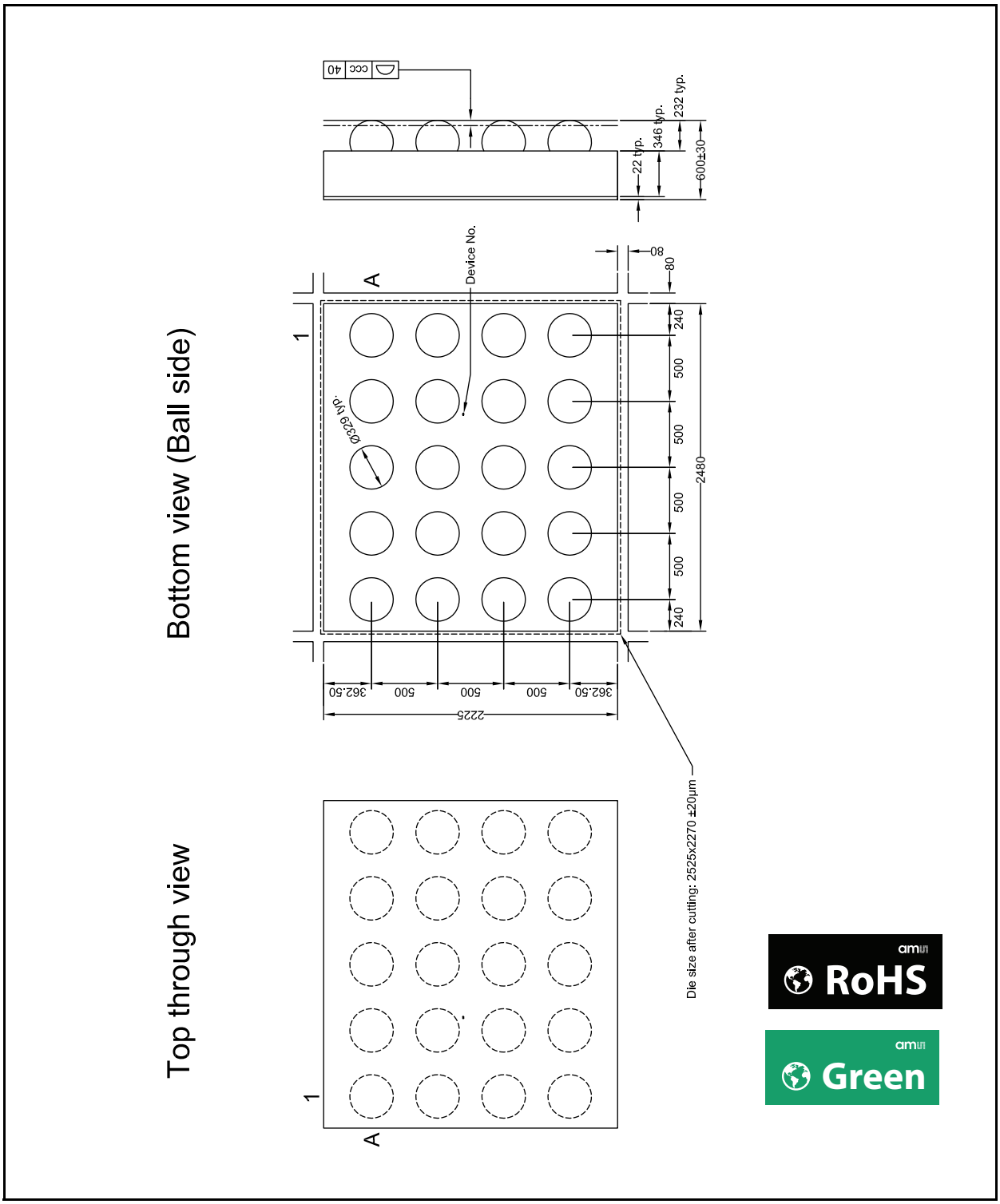
Assume that following conditions are set in the registers: PWM = 256, scan-limit = 5 (half filled matrix, 66 LEDs), I_{SEG} = 30mA

(EQ5)

$$I_{LEDavg} = 30mA \times \frac{256}{(5 + 1) \times 256} = 5mA$$

Package Drawings & Markings

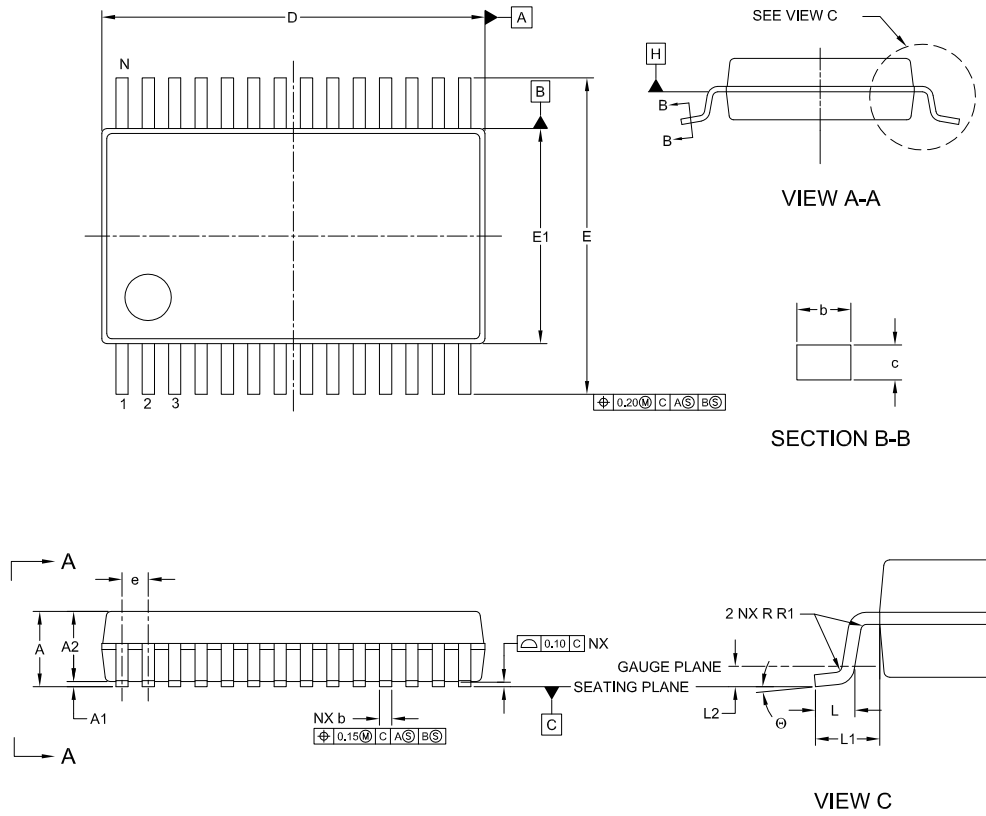
Figure 57:
20-Pin WL-CSP Package



Note(s):

1. Pin1= A1
2. ccc coplanarity
3. All dimensions are in µm.

Figure 58:
28-Pin SSOP Package



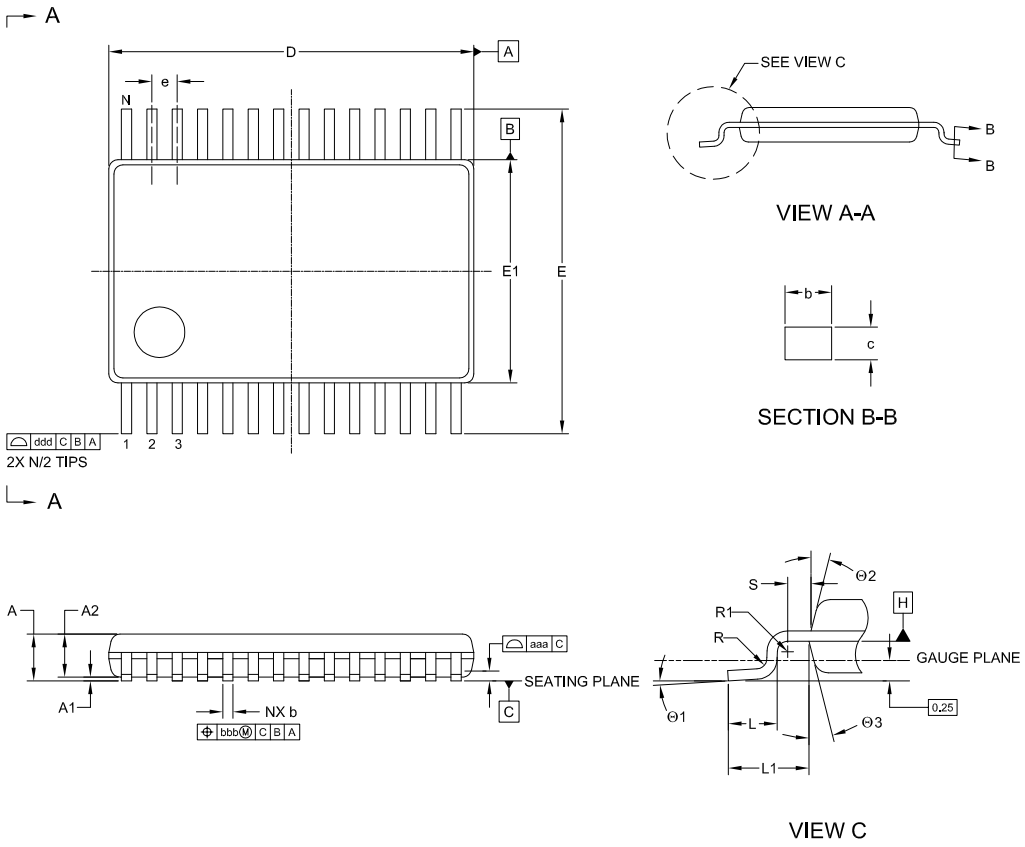
REF	MIN	NOM	MAX
A	1.73	1.86	1.99
A1	0.05	0.13	0.21
A2	1.68	1.73	1.78
b	0.22	0.30	0.38
c	0.09	0.17	0.25
D	9.90	10.20	10.50
E	7.40	7.80	8.20

REF	MIN	NOM	MAX
E1	5.00	5.30	5.60
e		0.65 BSC	
L	0.55	0.75	0.95
L1		1.25 REF	
L2		0.25 BSC	
R	0.09	-	-
Θ	0°	4°	8°
N		28	

Note(s):

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters, angles in degrees.
3. N is the total number of terminals.

Figure 59:
28-Pin TSSOP Package



REF	MIN	NOM	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	9.60	9.70	9.80
E	6.40 BSC		
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		

REF	MIN	NOM	MAX
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
Θ1	0°	-	8°
Θ2	12 REF		
Θ3	12 REF		
aaa	-	0.10	-
bbb	-	0.10	-
ccc	-	0.05	-
ddd	-	0.20	-
N	28		

Note(s):

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters, angles in degrees.
3. N is the total number of terminals.

Figure 60:
20-Pin WL-CSP Marking

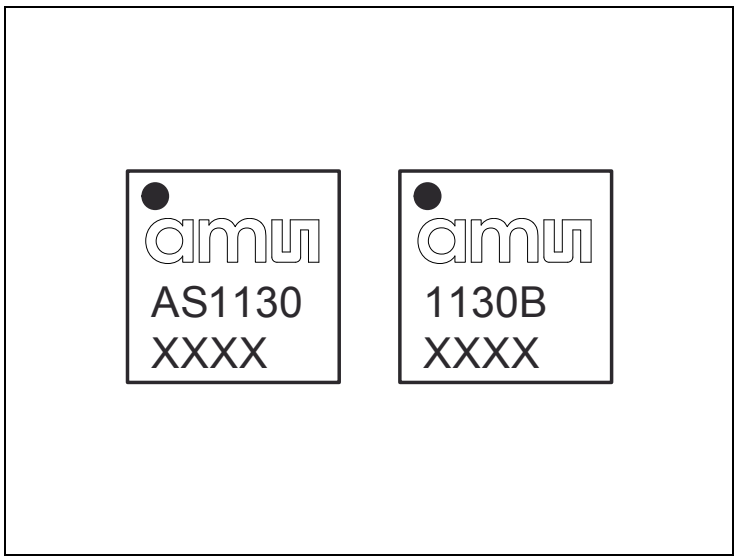


Figure 61:
Packaging Code XXXX

XXXX
Tracecode

Figure 62:
28-Pin SSOP Marking

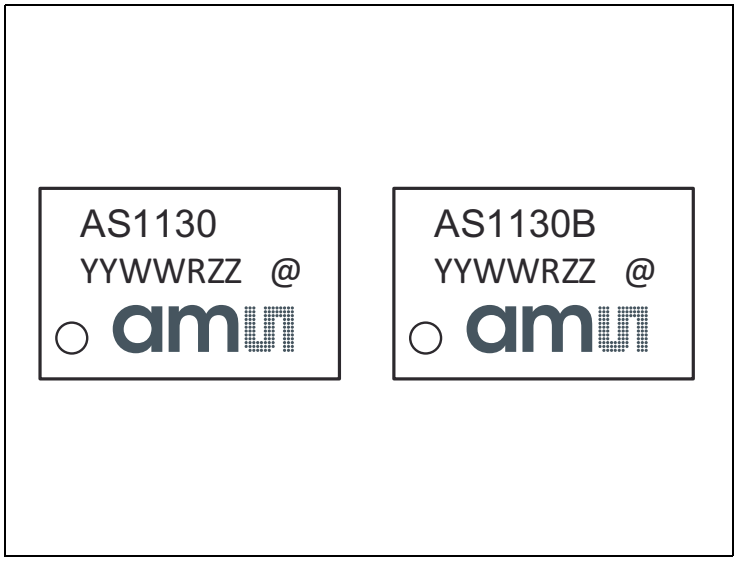


Figure 63:
28-Pin TSSOP Marking

Figure 64:
Packaging Code YYWWRZZ

YY	WW	R	ZZ	@
Last two digits of the manufacturing year	Manufacturing week	Plant identifier	Free choice / traceability code	Sublot identifier

Ordering & Contact Information

The devices are available as the standard products shown in Figure 65.

Figure 65:
Ordering Information

Ordering Code	Package	Marking	Description	Logic Levels	Address	Delivery Form
AS1130-BSST	28-pin SSOP	AS1130	132-LED Cross-Plexing Driver with Scrolling Function	CMOS	0x30 - 0x37	Tape and Reel
AS1130B-BSST(1)		AS1130B	132-LED Cross-Plexing Driver with Scrolling Function	Mobile		Tape and Reel
AS1130C-BSST(1)		AS1130C	132-LED Cross-Plexing Driver with Scrolling Function	CMOS	0x38 - 0x3E	Tape and Reel
AS1130D-BSST(1)		AS1130D	132-LED Cross-Plexing Driver with Scrolling Function	Mobile		Tape and Reel
AS1130-BTST	28-pin TSSOP	AS1130	132-LED Cross-Plexing Driver with scrolling Function	CMOS	0x30 - 0x37	Tape and Reel
AS1130B-BTST(1)		AS1130B	132-LED Cross-Plexing Driver with scrolling Function	Mobile		Tape and Reel
AS1130C-BTST(1)		AS1130C	132-LED Cross-Plexing Driver with scrolling Function	CMOS	0x38 - 0x3E	Tape and Reel
AS1130D-BTST(1)		AS1130D	132-LED Cross-Plexing Driver with scrolling Function	Mobile		Tape and Reel
AS1130-BWLT	20-Pin WL-CSP	AS1130	132-LED Cross-Plexing Driver with Scrolling Function	CMOS	0x30 - 0x37	Tape and Reel
AS1130B-BWLT		AS1130B	132-LED Cross-Plexing Driver with Scrolling Function	Mobile		Tape and Reel
AS1130C-BWLT(1)		tbd	132-LED Cross-Plexing Driver with Scrolling Function	CMOS	0x38 - 0x3E	Tape and Reel
AS1130D-BWLT(1)		tbd	132-LED Cross-Plexing Driver with Scrolling Function	Mobile		Tape and Reel

Note(s):

1. On request

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Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Revision Information

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Updated Figure 60	58

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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